OIPE JC106
MAY 25 2005
PATENT & TRADEMARK OFFICE

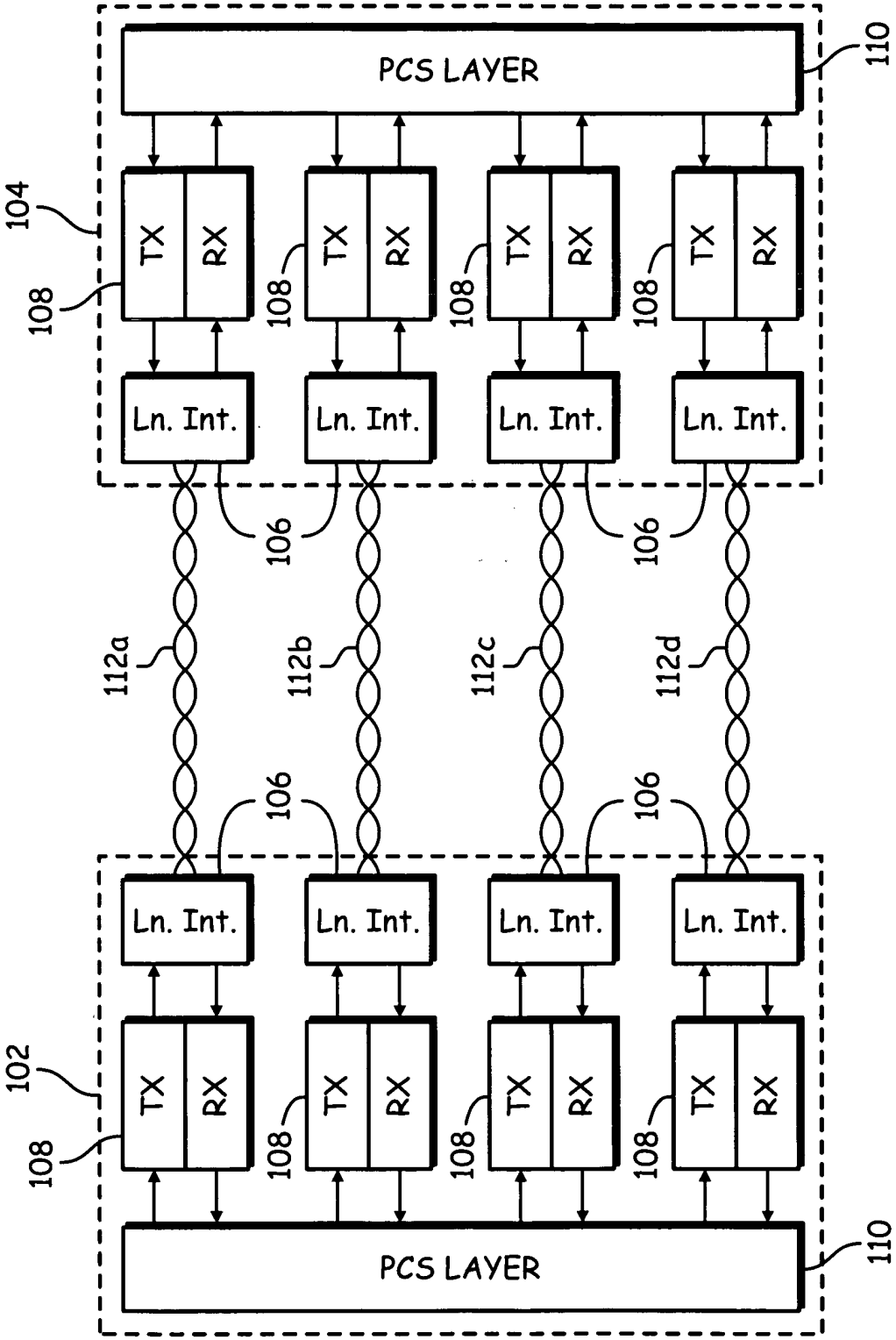


FIG. 1

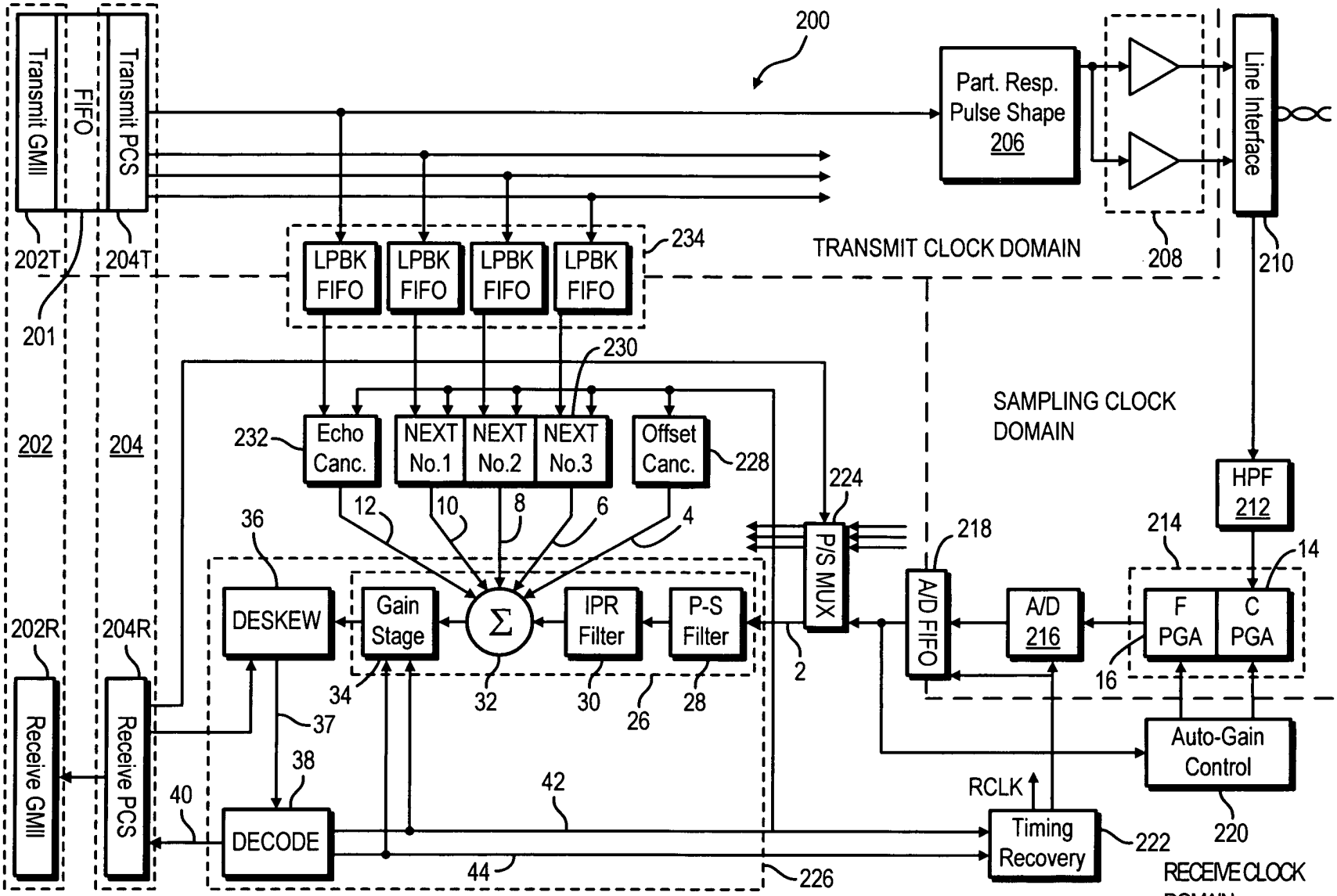

200
Transmit GMII
FIFO
Transmit PCS
202T
204T
201
Part. Resp. Pulse Shape 206
Line Interface
208
210
TRANSMIT CLOCK DOMAIN
LPBK FIFO
LPBK FIFO
LPBK FIFO
LPBK FIFO
234
230
SAMPLING CLOCK DOMAIN
202
204
232
Echo Canc.
NEXT No.1
NEXT No.2
NEXT No.3
Offset Canc.
228
224
HPF 212
214
14
12
10
8
6
4
36
218
P/S MUX
A/D FIFO
A/D 216
F PGA
C PGA
16
DESKEW
Gain Stage
Σ
IPR Filter
P-S Filter
2
202R
204R
34
32
30
26
28
Receive GMII
Receive PCS
37
Auto-Gain Control
38
RCLK
42
40
DECODE
Timing Recovery
222
220
44
226
RECEIVE CLOCK DOMAIN

FIG. 2

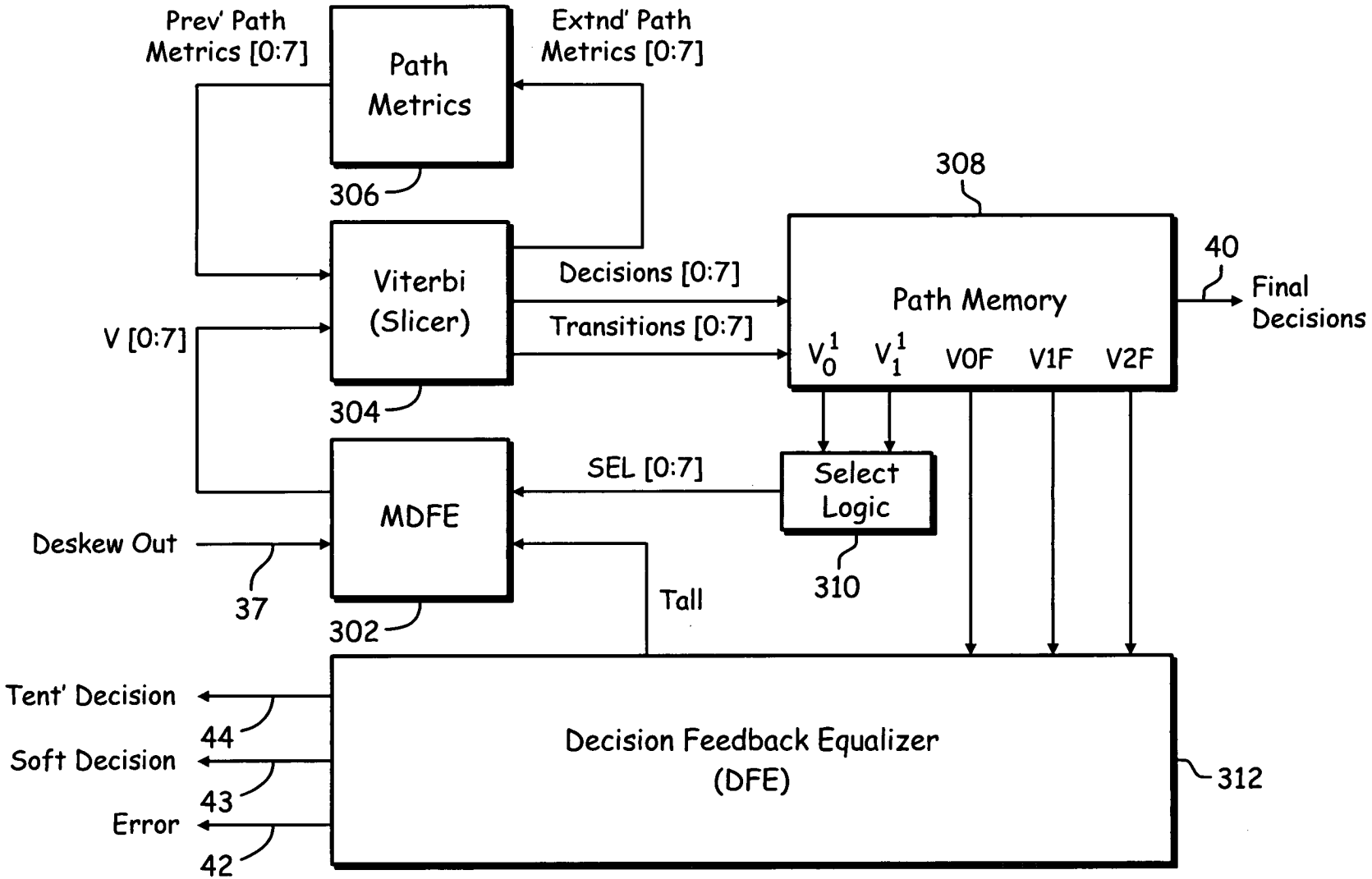

Prev' Path Metrics [0:7]
Path Metrics
Extnd' Path Metrics [0:7]
306
308
Viterbi (Slicer)
Decisions [0:7]
Transitions [0:7]
Path Memory
40
Final Decisions
V [0:7]
V_0^1 V_1^1 V0F V1F V2F
304
SEL [0:7]
Select Logic
MDFE
Deskew Out
37
310
Tall
302
Tent' Decision
44
Soft Decision
43
Error
42
Decision Feedback Equalizer (DFE)
312

FIG. 3

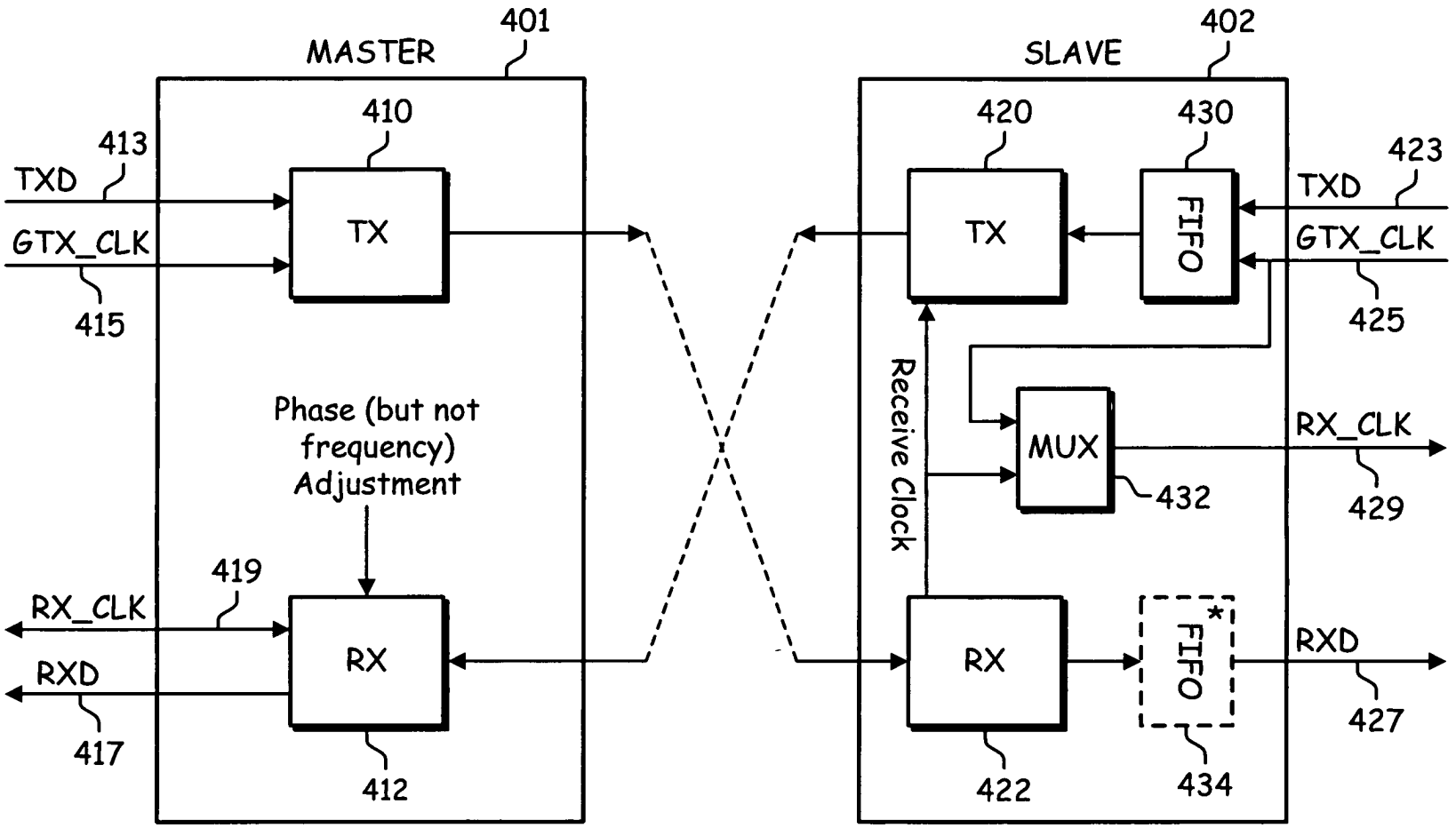

MASTER
401
SLAVE
402
410
420
430
413
TXD
TX
TX
FIFO
423
TXD
GTX_CLK
GTX_CLK
415
425
Receive Clock
Phase (but not frequency) Adjustment
MUX
RX_CLK
432
429
419
RX_CLK
RX
RX
FIFO
*
RXD
RXD
417
427
412
422
434

FIG. 4

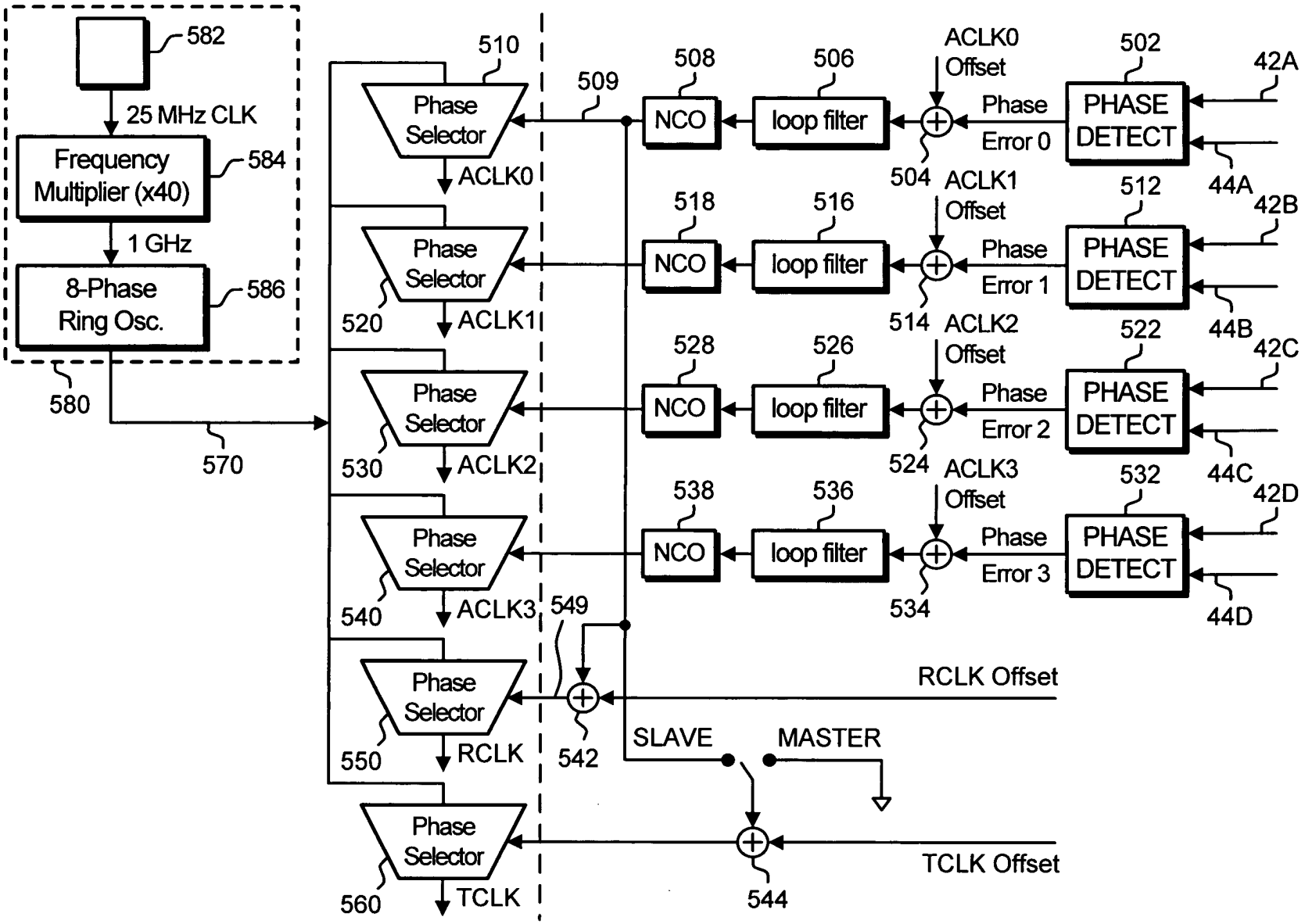

582
25 MHz CLK
Frequency Multiplier (x40)
584
1 GHz
8-Phase Ring Osc.
586
580
570
510
509
508
506
ACLK0 Offset
502
42A
Phase Selector
NCO
loop filter
Phase Error 0
PHASE DETECT
ACLK0
504
44A
518
516
ACLK1 Offset
512
42B
Phase Selector
NCO
loop filter
Phase Error 1
PHASE DETECT
520
ACLK1
514
44B
528
526
ACLK2 Offset
522
42C
Phase Selector
NCO
loop filter
Phase Error 2
PHASE DETECT
530
ACLK2
524
44C
538
536
ACLK3 Offset
532
42D
Phase Selector
NCO
loop filter
Phase Error 3
PHASE DETECT
540
ACLK3
534
44D
549
RCLK Offset
Phase Selector
550
RCLK
542
SLAVE
MASTER
Phase Selector
560
TCLK
544
TCLK Offset

FIG. 5

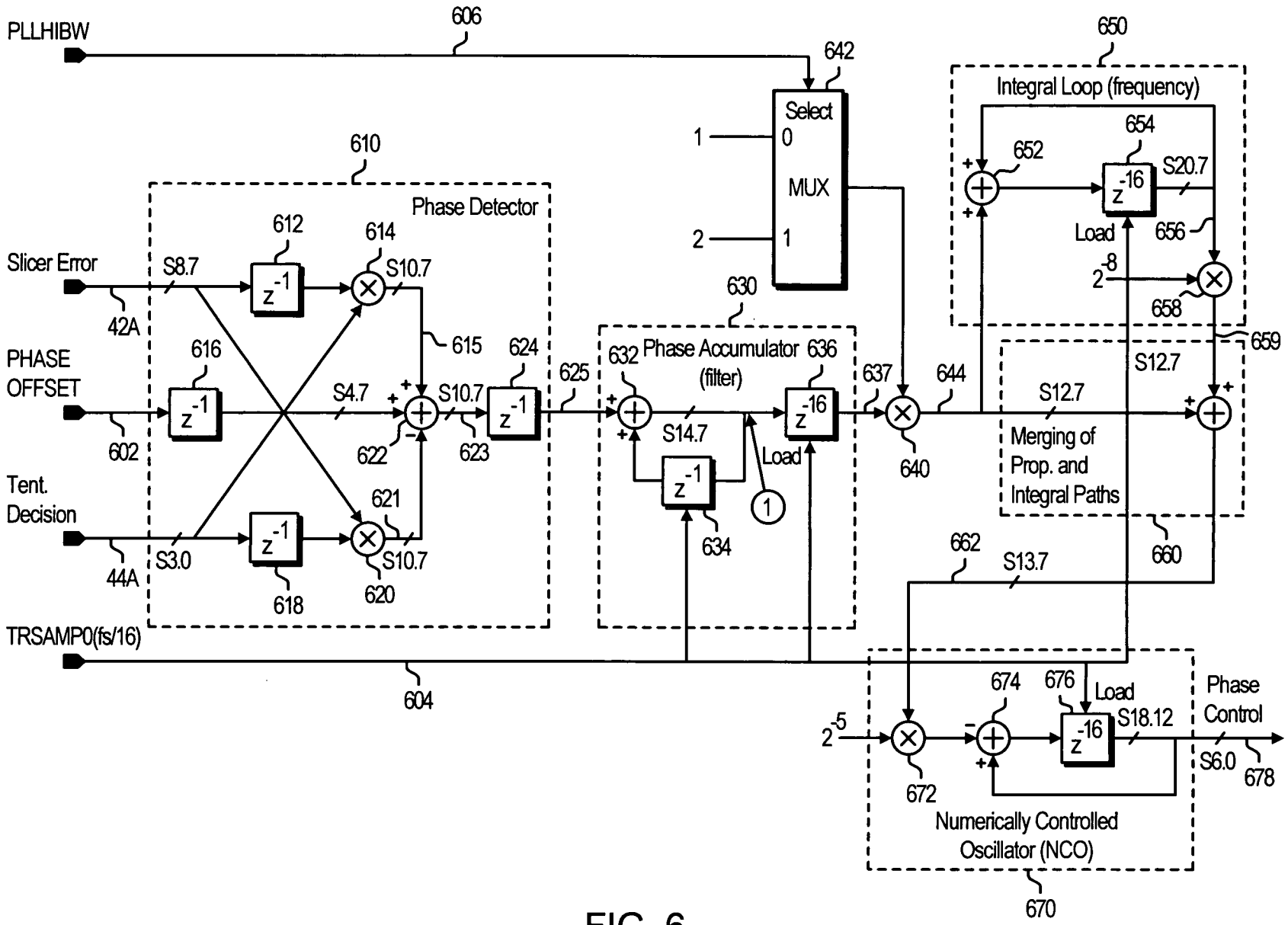

PLLHIBW
606
642
650
Integral Loop (frequency)
Select
1
0
MUX
2
1
610
Phase Detector
654
652
S20.7
Load
656
658
659
Slicer Error
S8.7
612
614
S10.7
42A
615
624
630
632
Phase Accumulator
(filter)
636
637
644
S12.7
PHASE
OFFSET
616
S4.7
625
S14.7
Load
640
Merging of
Prop. and
Integral Paths
602
622
623
634
660
Tent.
Decision
621
662
S13.7
S3.0
S10.7
44A
618
620
TRSAMP0(fs/16)
604
674
676
Load
S18.12
Phase
Control
S6.0
678
672
Numerically Controlled
Oscillator (NCO)
670

FIG. 6

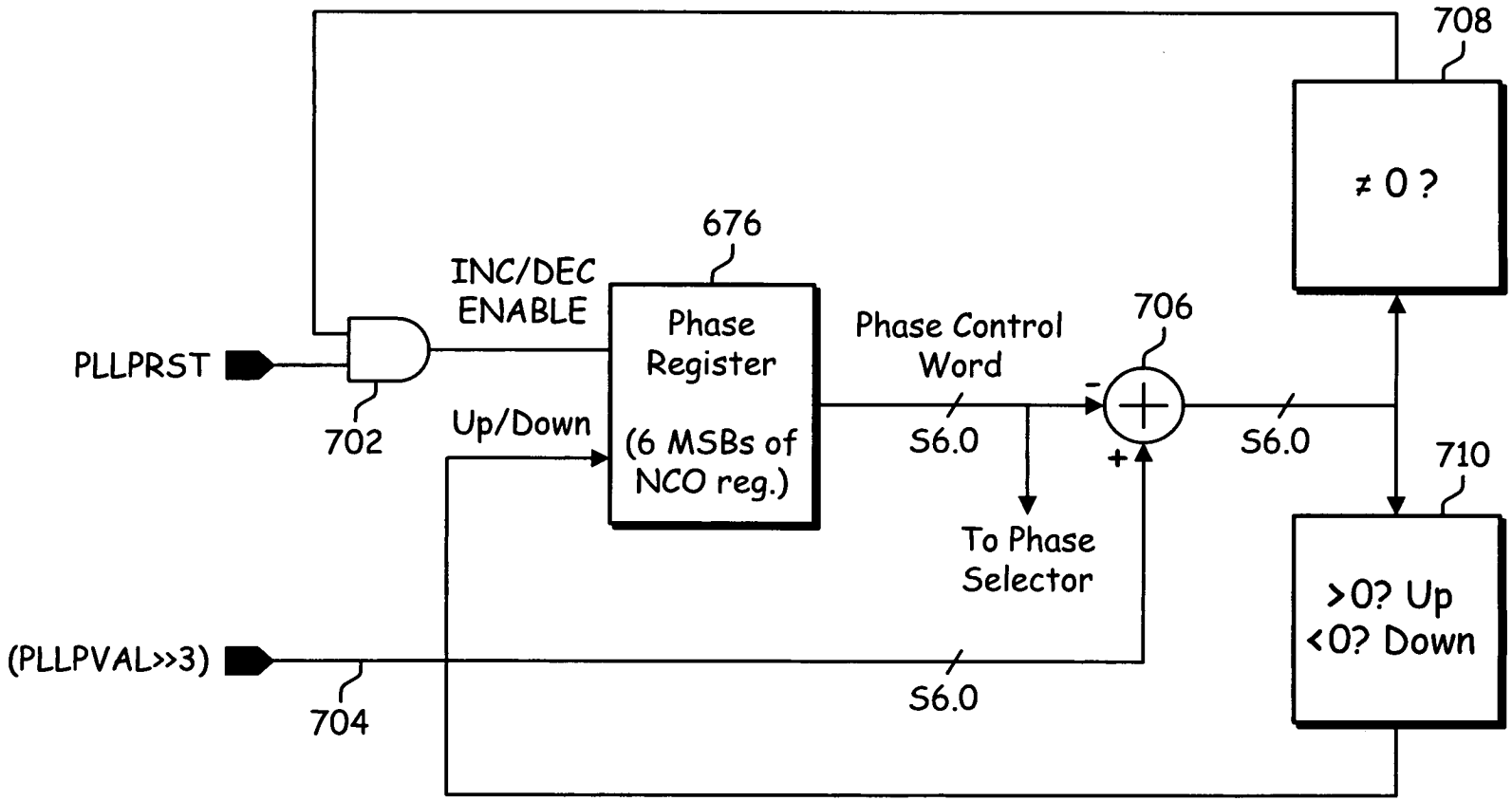

708
≠ 0 ?
676
INC/DEC
ENABLE
Phase
Register
(6 MSBs of
NCO reg.)
Phase Control
Word
706
PLLPRST
702
Up/Down
S6.0
S6.0
710
To Phase
Selector
>0? Up
<0? Down
(PLLPVAL>>3)
704
S6.0

FIG. 7

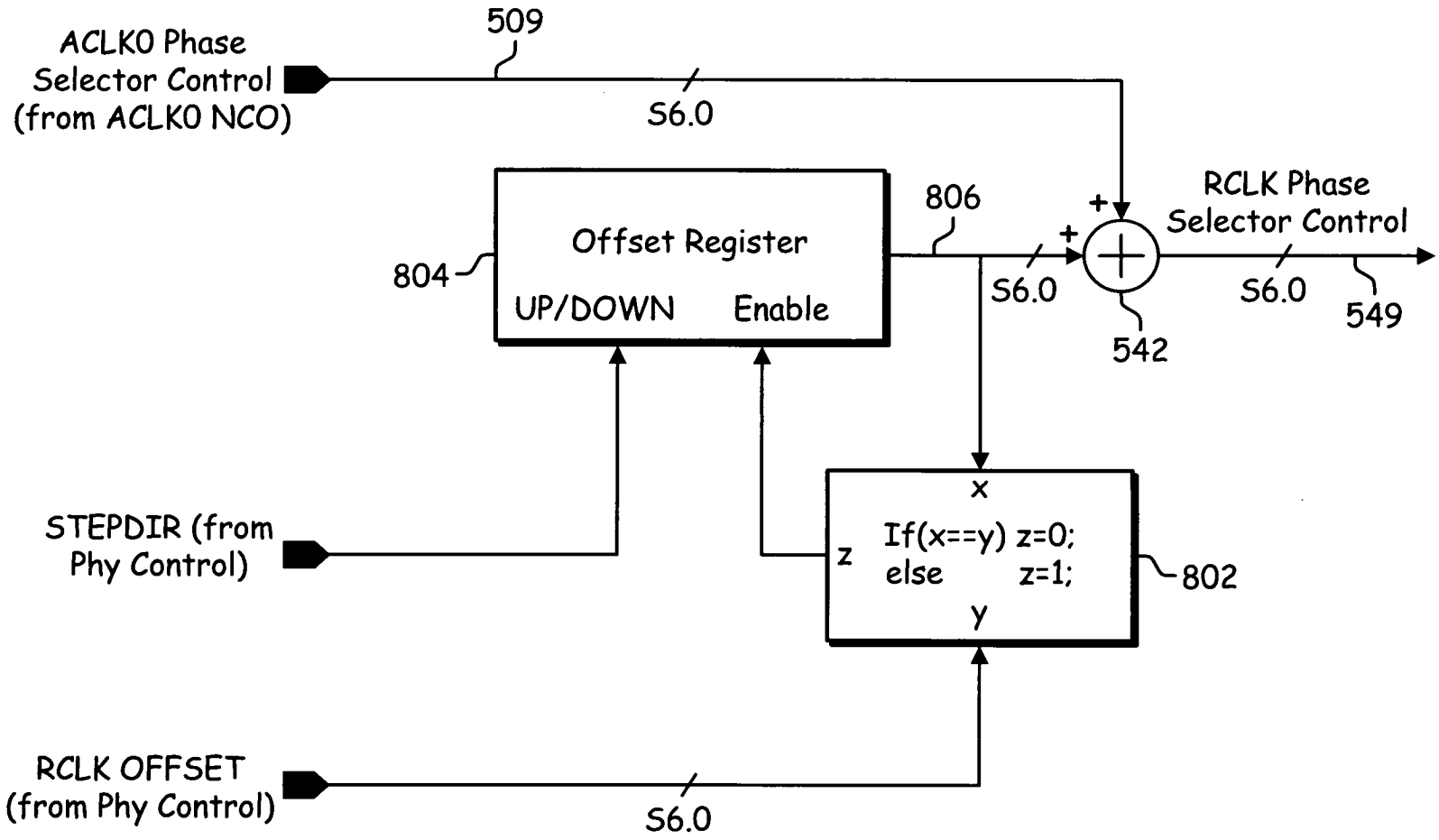

ACLK0 Phase
Selector Control
(from ACLK0 NCO)
509
S6.0
Offset Register
UP/DOWN
Enable
804
806
S6.0
+
+
RCLK Phase
Selector Control
S6.0
549
542
STEPDIR (from
Phy Control)
x
z
If(x==y) z=0;
else z=1;
y
802
RCLK OFFSET
(from Phy Control)
S6.0

FIG. 8

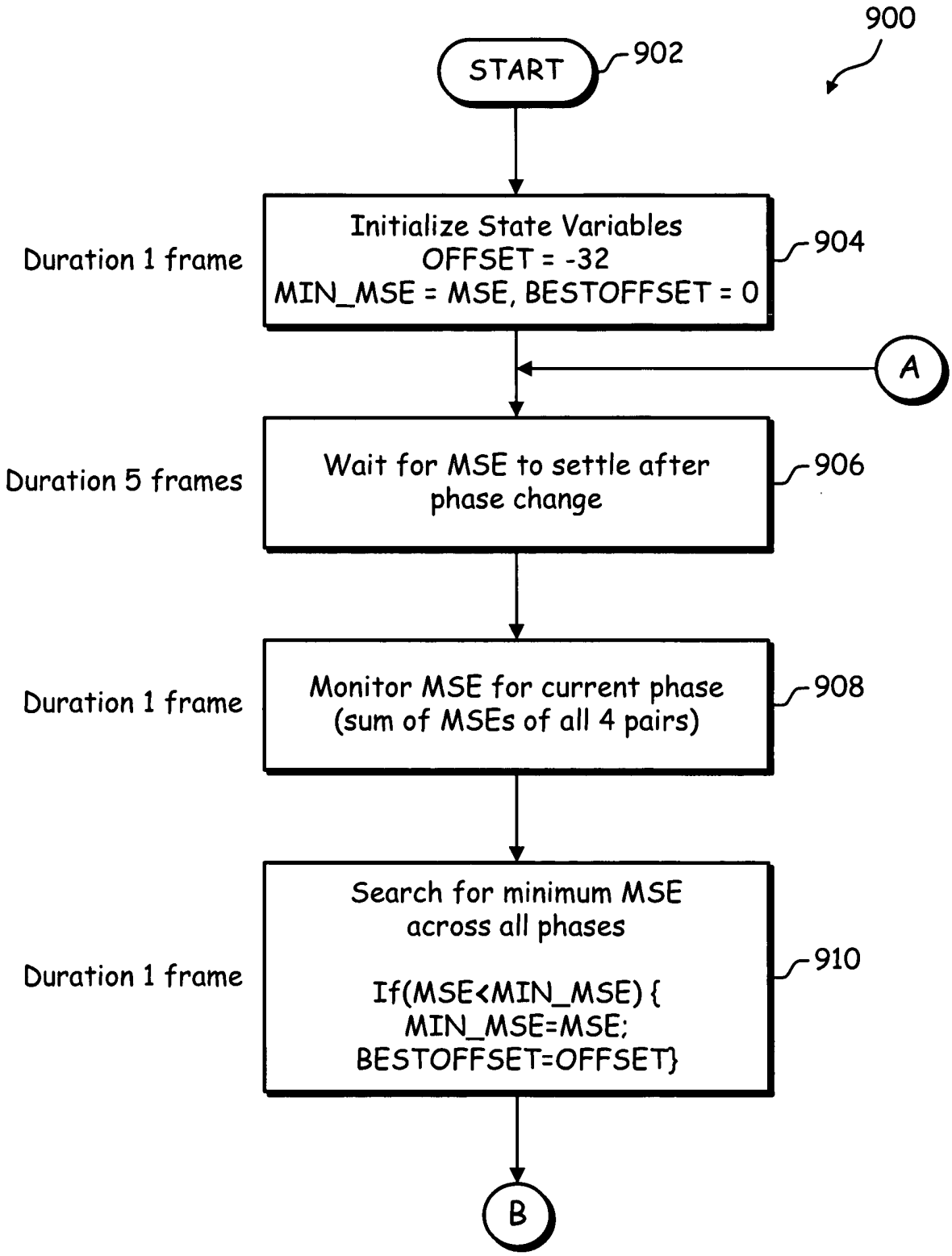

900
START
902
Initialize State Variables
OFFSET = -32
MIN_MSE = MSE, BESTOFFSET = 0
904
Duration 1 frame
A
Wait for MSE to settle after
phase change
906
Duration 5 frames
Monitor MSE for current phase
(sum of MSEs of all 4 pairs)
908
Duration 1 frame
Search for minimum MSE
across all phases
If(MSE<MIN_MSE) {
MIN_MSE=MSE;
BESTOFFSET=OFFSET}
910
Duration 1 frame
B

FIG. 9a

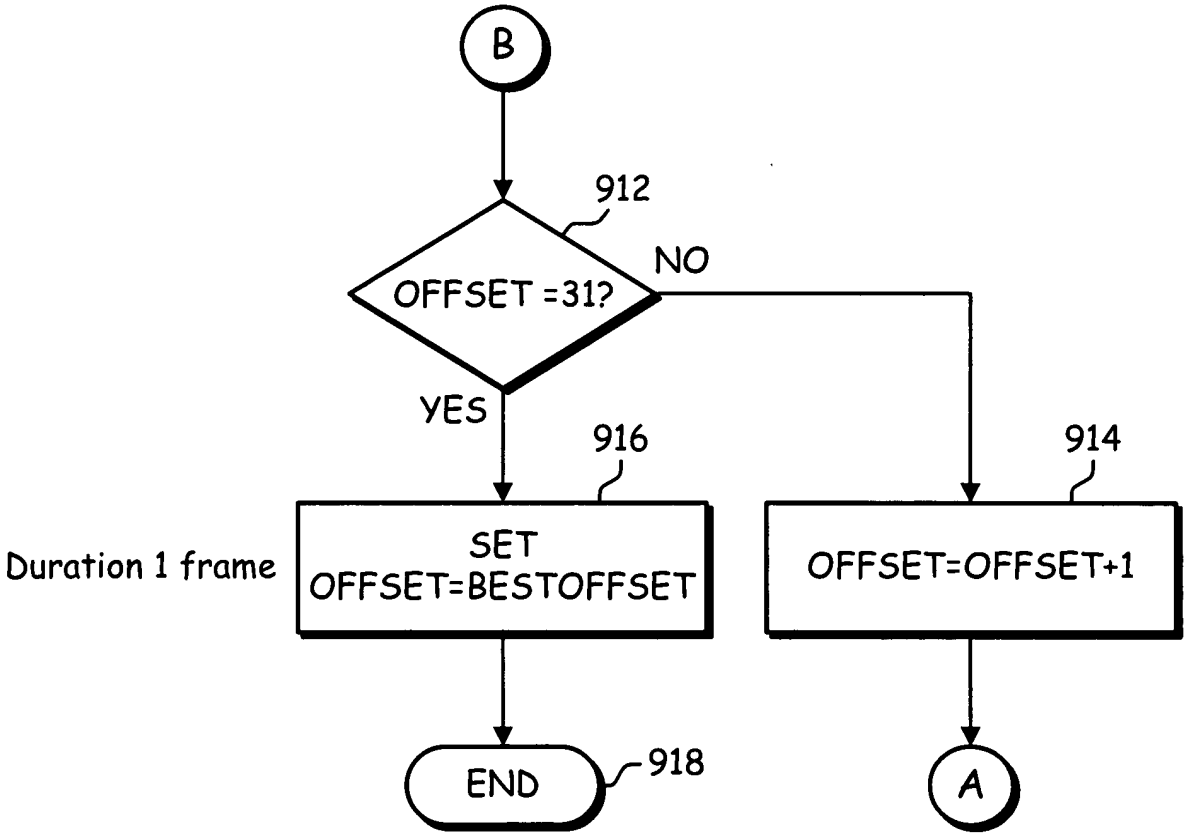

B
912
OFFSET =31?
NO
YES
916
914
Duration 1 frame
SET
OFFSET=BESTOFFSET
OFFSET=OFFSET+1
END
918
A

FIG. 9b

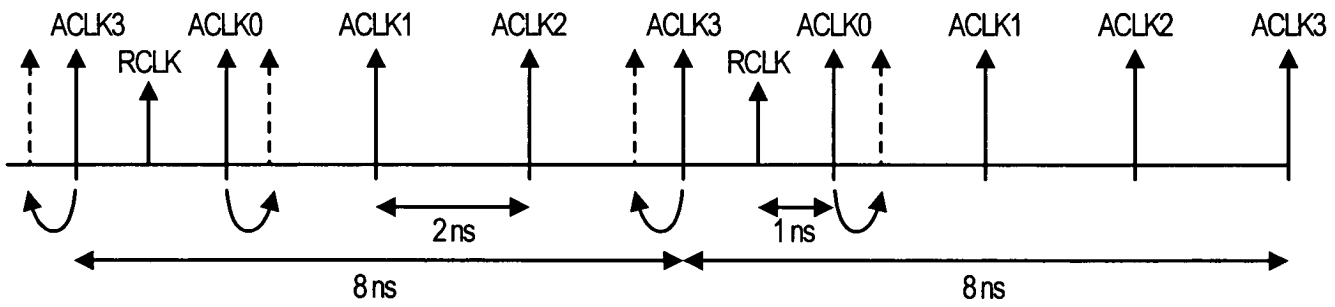


FIG. 10a

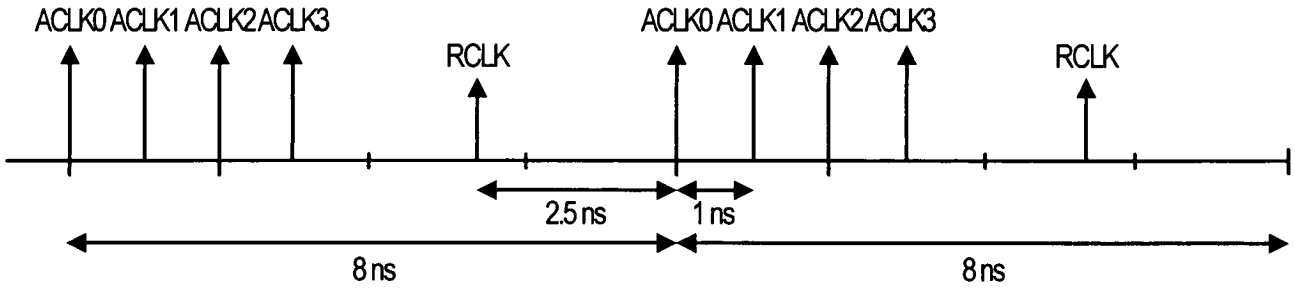


FIG. 10b

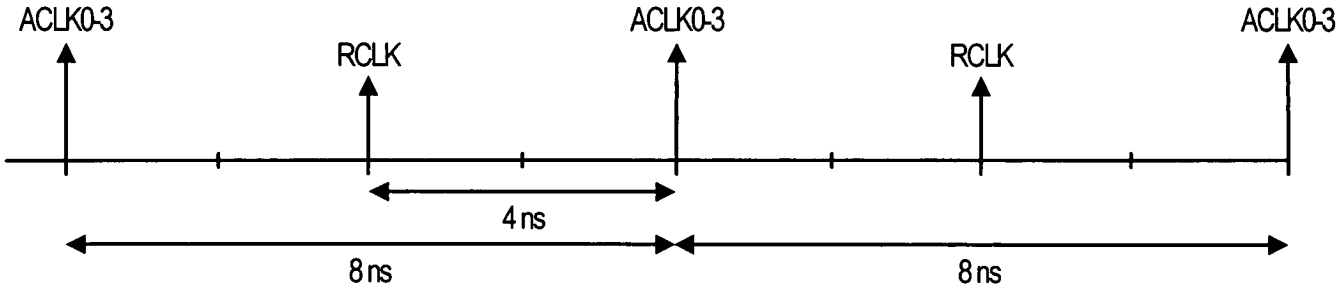


FIG. 10c

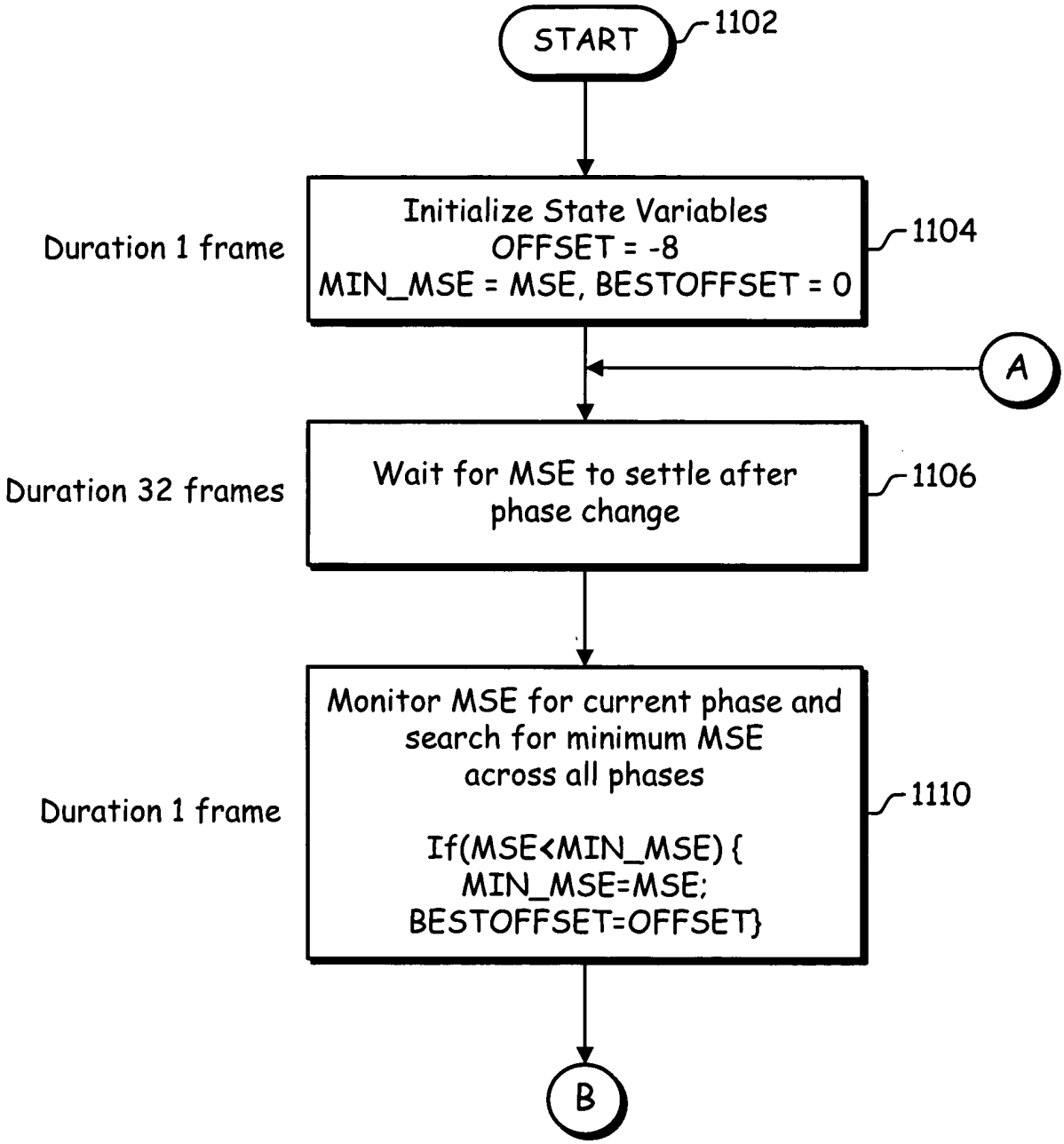

START
1102
Initialize State Variables
OFFSET = -8
MIN_MSE = MSE, BESTOFFSET = 0
1104
Duration 1 frame
A
Wait for MSE to settle after
phase change
1106
Duration 32 frames
Monitor MSE for current phase and
search for minimum MSE
across all phases
If(MSE<MIN_MSE) {
MIN_MSE=MSE;
BESTOFFSET=OFFSET}
1110
Duration 1 frame
B

FIG. 11a

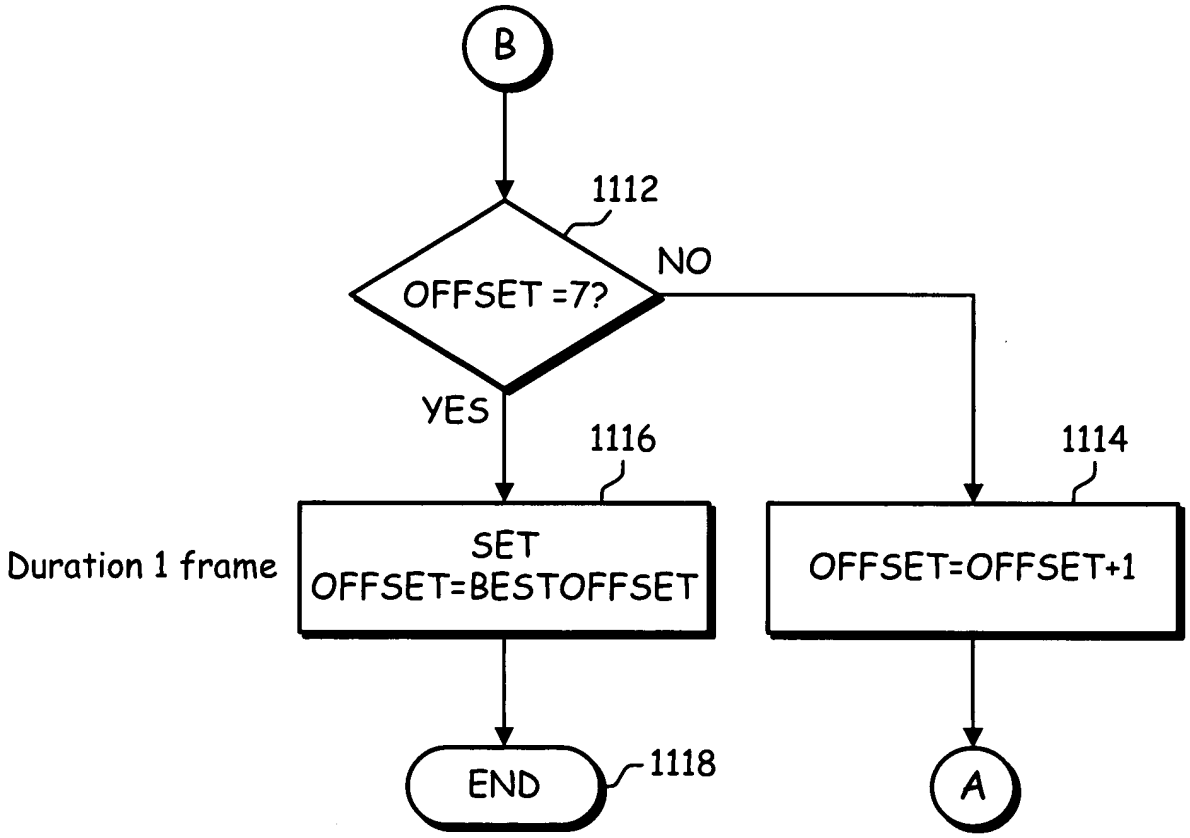

B
1112
OFFSET =7?
NO
YES
1116
1114
Duration 1 frame
SET
OFFSET=BESTOFFSET
OFFSET=OFFSET+1
END
1118
A

FIG. 11b

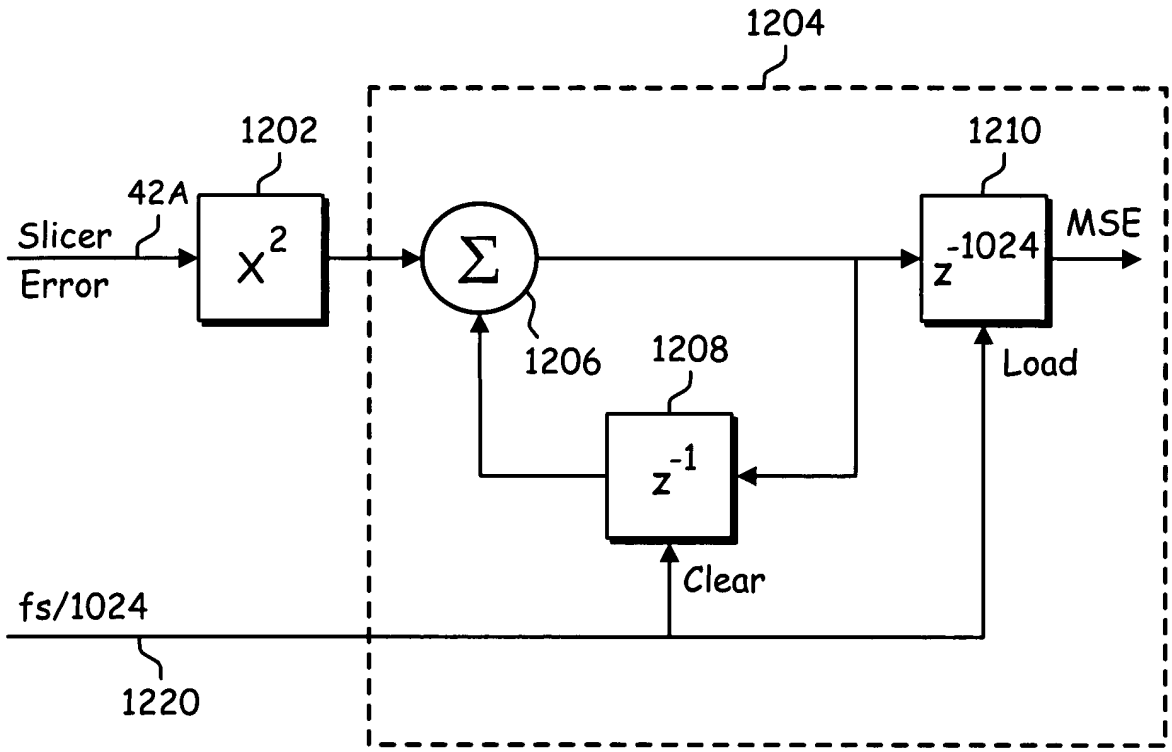

1204
1202
1210
42A
Slicer
Error
X^2
Σ
z^{-1024}
MSE
1206
1208
Load
z^{-1}
Clear
fs/1024
1220

FIG. 12

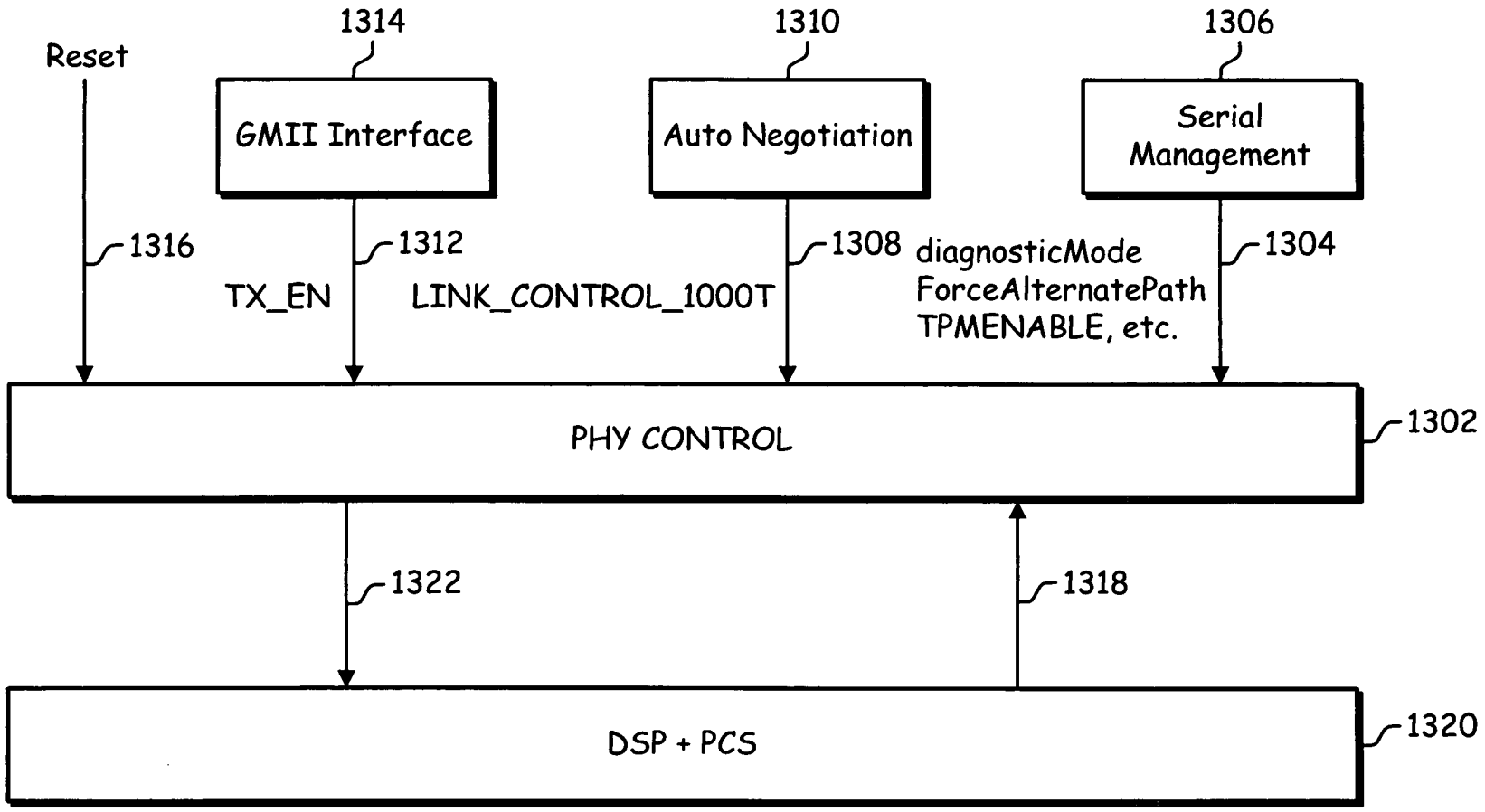

Reset
1314
GMII Interface
1310
Auto Negotiation
1306
Serial Management
1316
1312
TX_EN
LINK_CONTROL_1000T
1308
diagnosticMode
ForceAlternatePath
TPMENABLE, etc.
1304
PHY CONTROL
1302
1322
1318
DSP + PCS
1320

FIG. 13

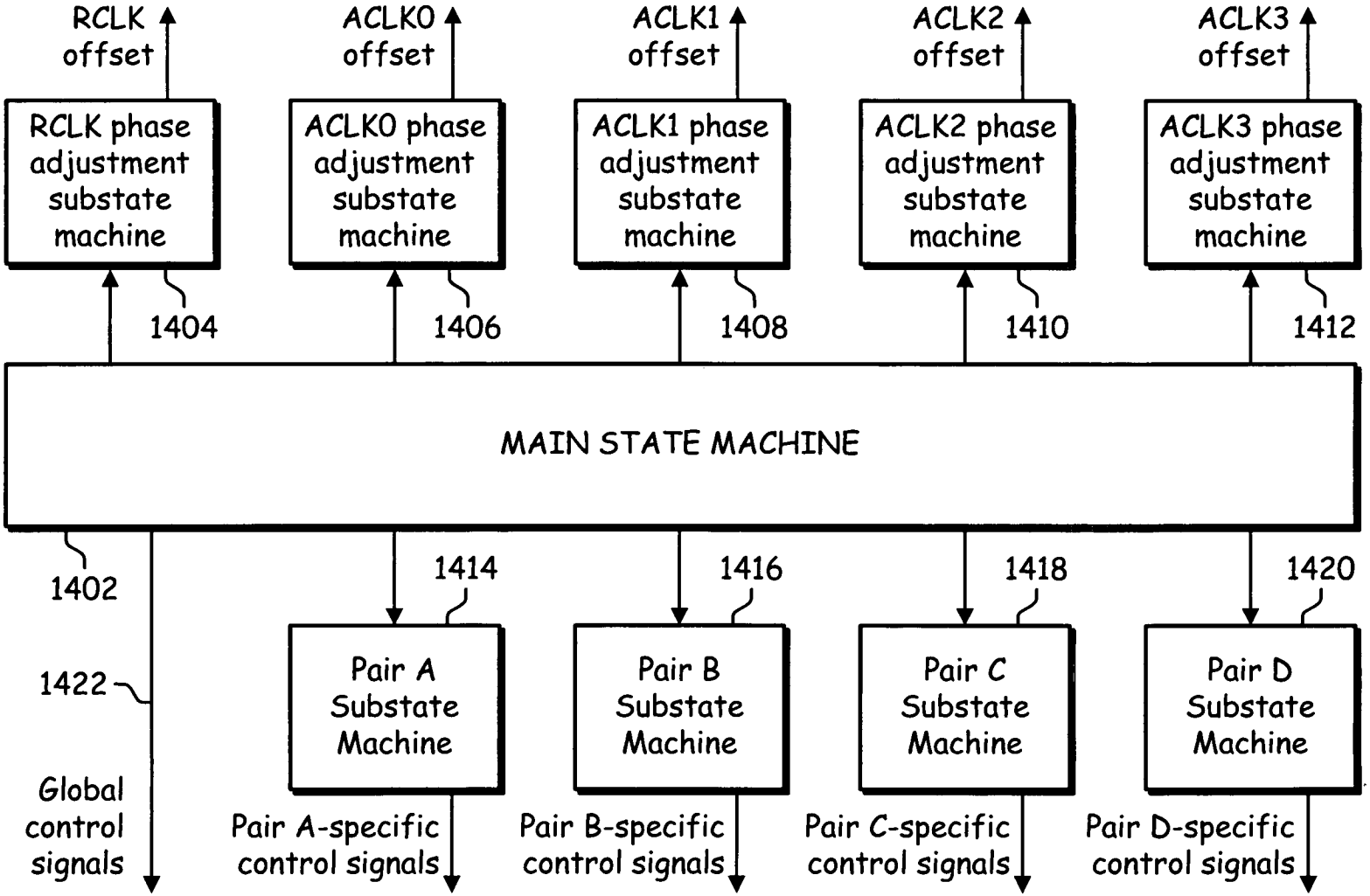
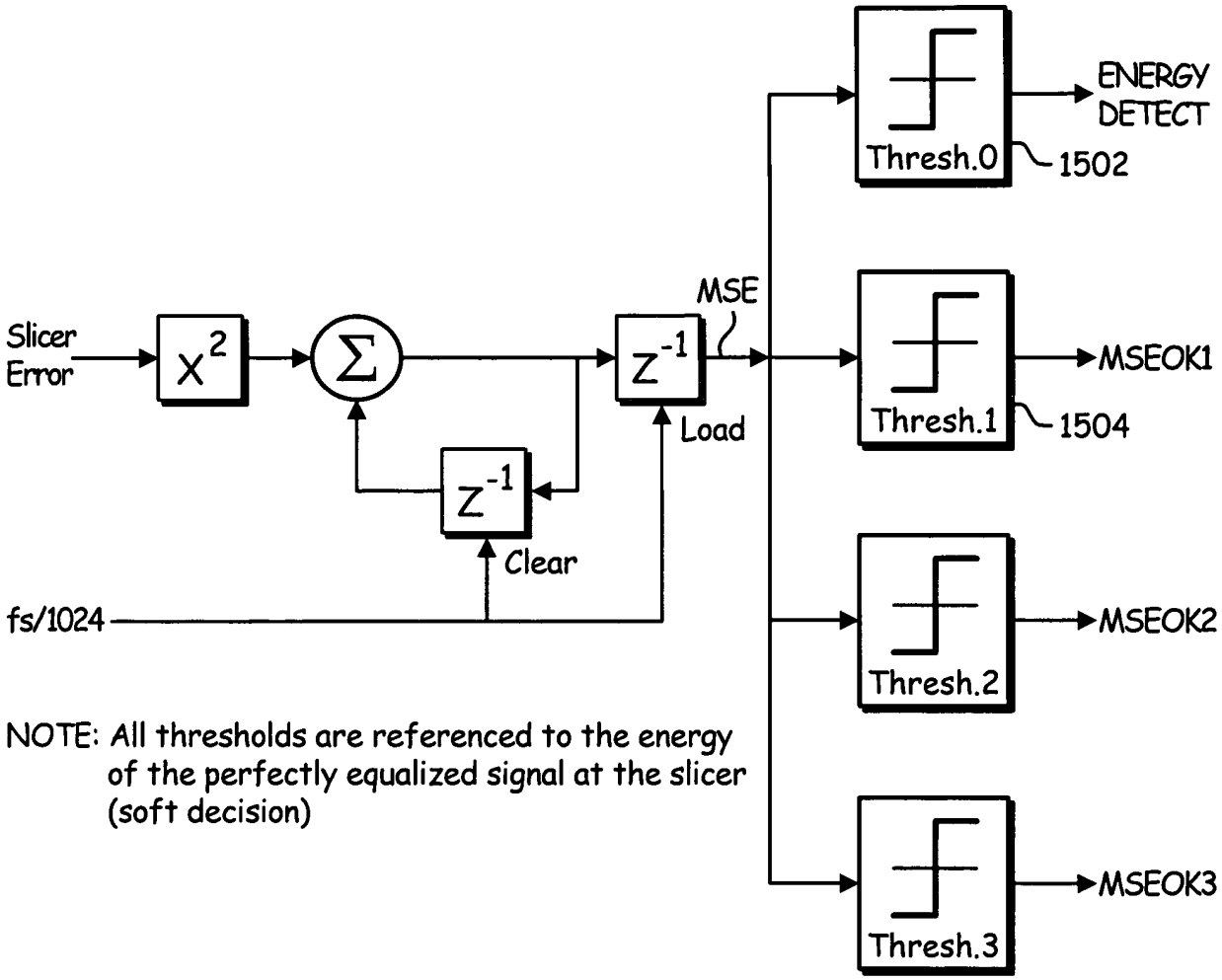

RCLK offset
ACLK0 offset
ACLK1 offset
ACLK2 offset
ACLK3 offset
RCLK phase adjustment substate machine
ACLK0 phase adjustment substate machine
ACLK1 phase adjustment substate machine
ACLK2 phase adjustment substate machine
ACLK3 phase adjustment substate machine
1404
1406
1408
1410
1412
MAIN STATE MACHINE
1402
1414
1416
1418
1420
1422
Pair A Substate Machine
Pair B Substate Machine
Pair C Substate Machine
Pair D Substate Machine
Global control signals
Pair A-specific control signals
Pair B-specific control signals
Pair C-specific control signals
Pair D-specific control signals

FIG. 14



NOTE: All thresholds are referenced to the energy of the perfectly equalized signal at the slicer (soft decision)

THRESHOLD	VALUE[dB]	FUNCTION
Thresh.0	-20	ENERGY DETECT
Thresh.1	-17	loc_rcvr_status_OK
Thresh.2	-12	frequency recovery
Thresh.3 (1)	-22.8 (SER=1e-13)	Quality Indicator
Thresh.3 (2)	-22.5 (SER=1e-12)	Quality Indicator
Thresh.3 (3)	-22.0 (SER=1e-11)	Quality Indicator (default)
Thresh.3 (4)	-21.5 (SER=1e-10)	Quality Indicator

FIG. 15

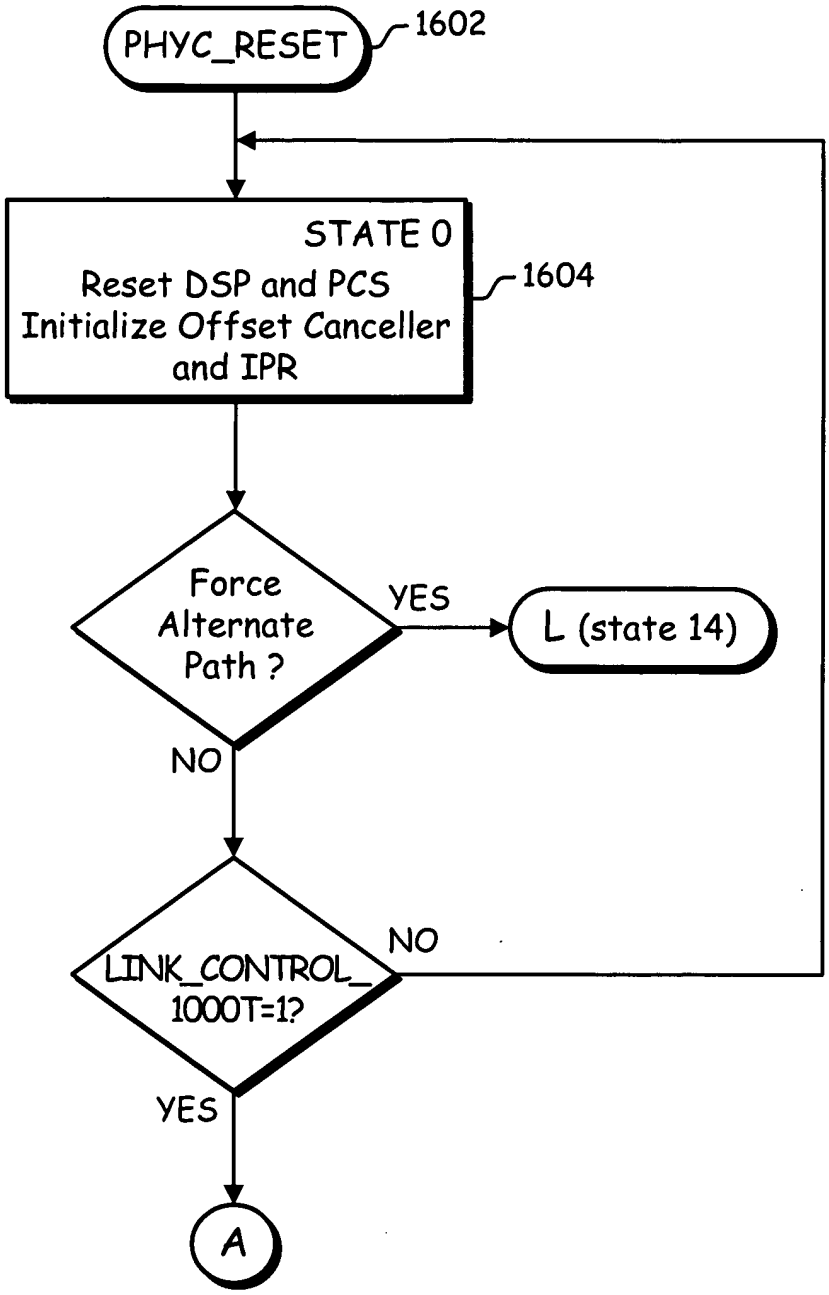

PHYC_RESET
1602
STATE 0
Reset DSP and PCS
Initialize Offset Canceller
and IPR
1604
Force
Alternate
Path ?
YES
L (state 14)
NO
LINK_CONTROL_
1000T=1?
NO
YES
A

FIG. 16A

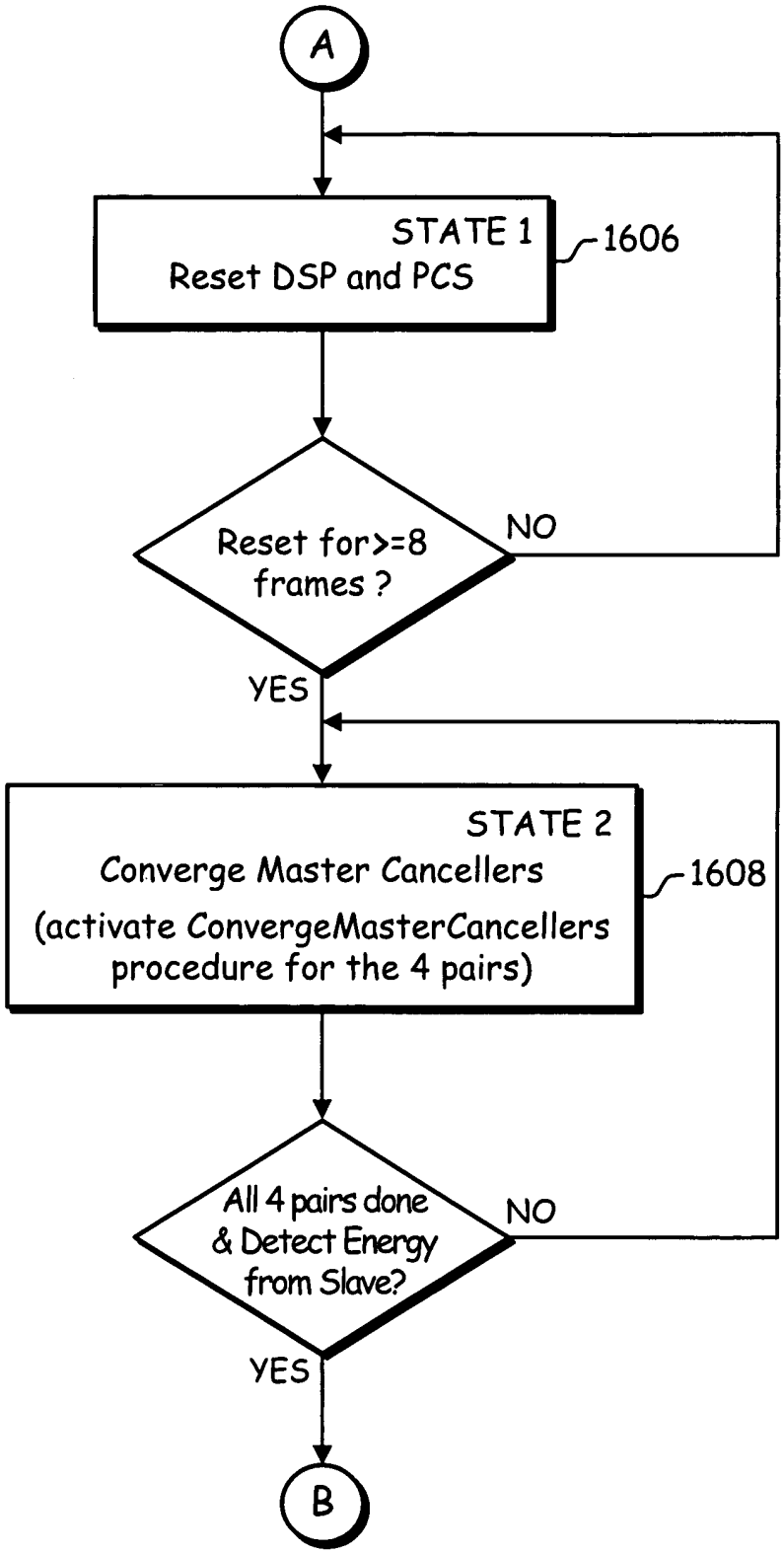

A
STATE 1
Reset DSP and PCS
1606
Reset for>=8 frames ?
NO
YES
STATE 2
Converge Master Cancellers
(activate ConvergeMasterCancellers procedure for the 4 pairs)
1608
All 4 pairs done & Detect Energy from Slave?
NO
YES
B

FIG. 16B

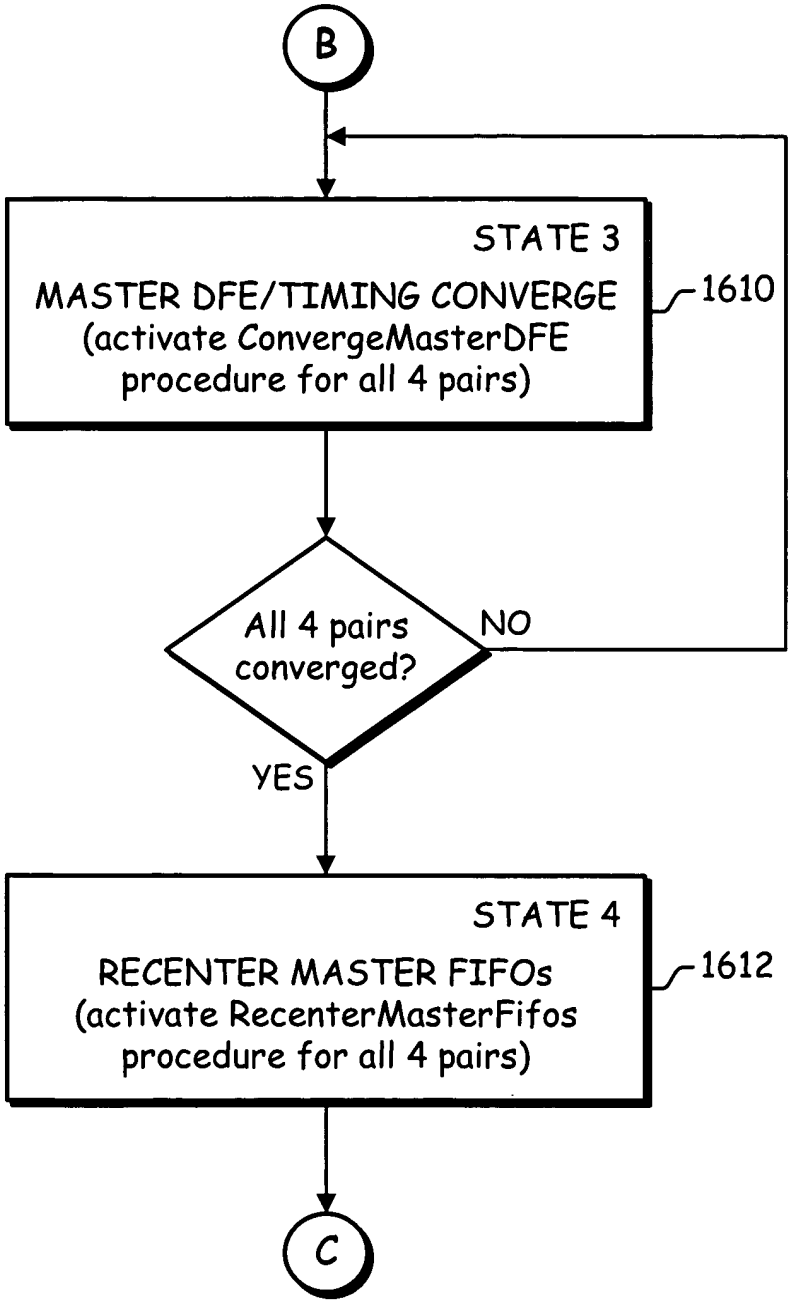

B
STATE 3
MASTER DFE/TIMING CONVERGE
(activate ConvergeMasterDFE
procedure for all 4 pairs)
1610
All 4 pairs
converged?
NO
YES
STATE 4
RECENTER MASTER FIFOs
(activate RecenterMasterFifos
procedure for all 4 pairs)
1612
C

FIG. 16C

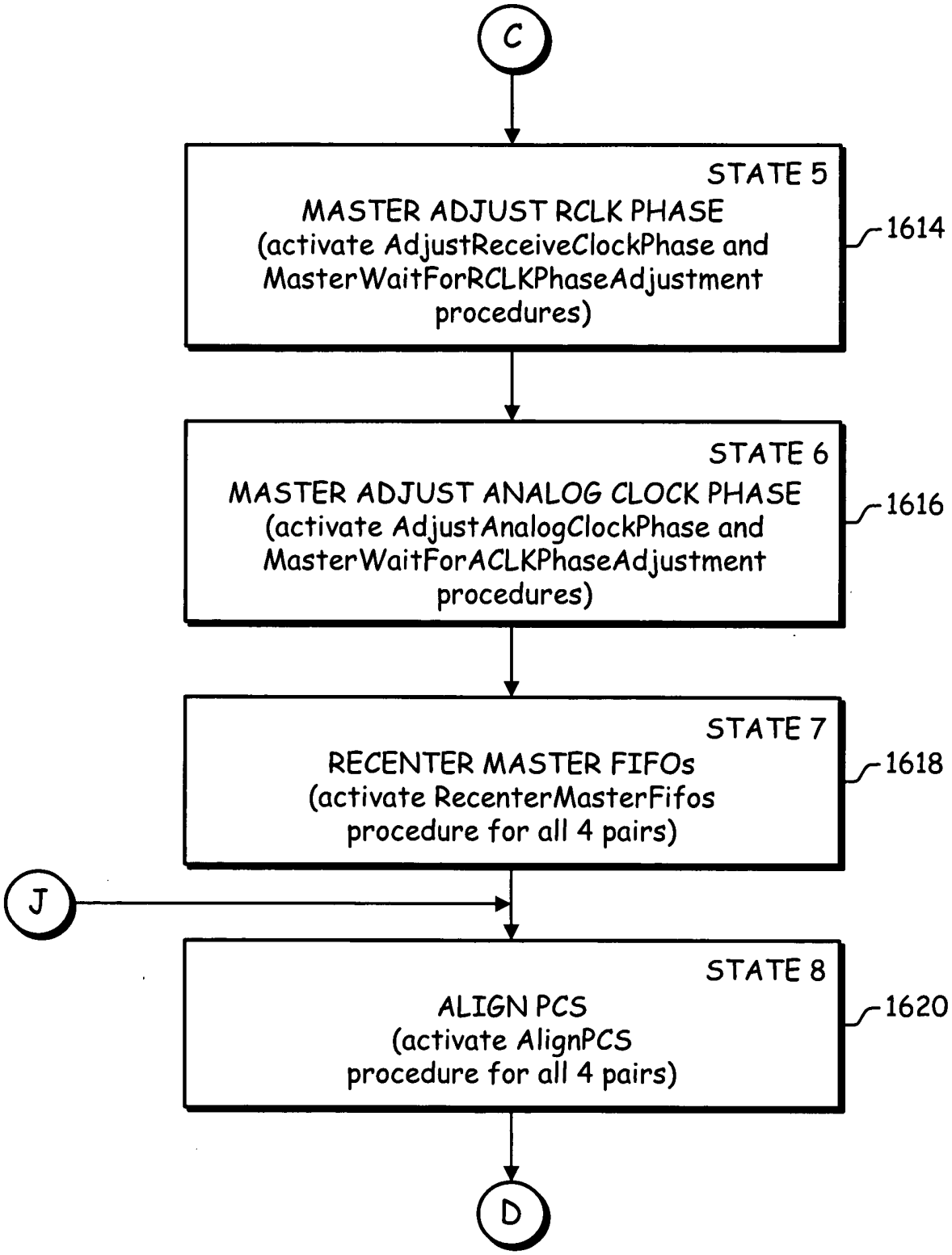

C
STATE 5
MASTER ADJUST RCLK PHASE
(activate AdjustReceiveClockPhase and
MasterWaitForRCLKPhaseAdjustment
procedures)
1614
STATE 6
MASTER ADJUST ANALOG CLOCK PHASE
(activate AdjustAnalogClockPhase and
MasterWaitForACLKPhaseAdjustment
procedures)
1616
STATE 7
RECENTER MASTER FIFOs
(activate RecenterMasterFifos
procedure for all 4 pairs)
1618
J
STATE 8
ALIGN PCS
(activate AlignPCS
procedure for all 4 pairs)
1620
D

FIG. 16D

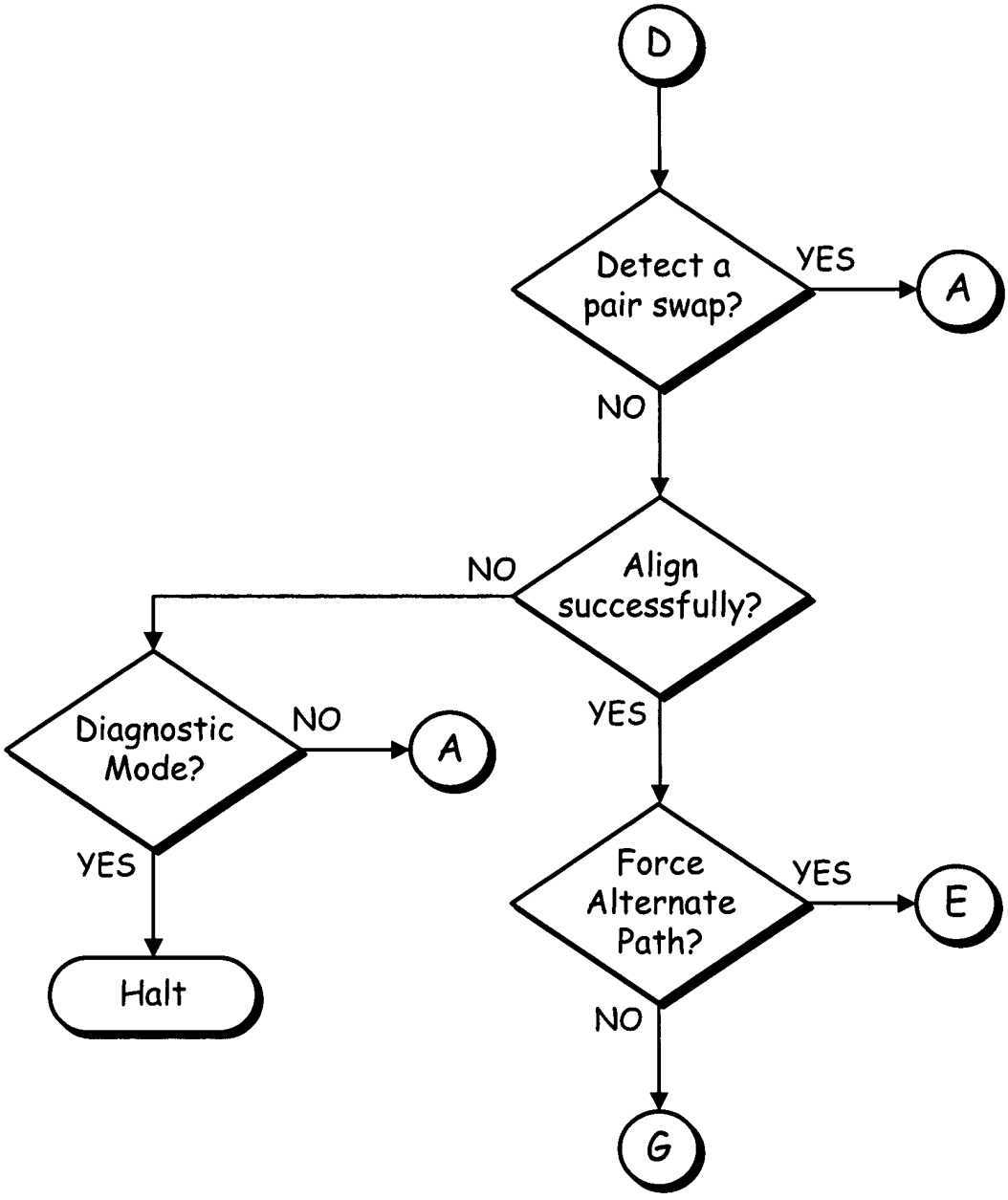

D
Detect a pair swap?
YES
A
NO
Align successfully?
NO
YES
Diagnostic Mode?
NO
A
YES
Halt
Force Alternate Path?
YES
E
NO
G

FIG. 16E

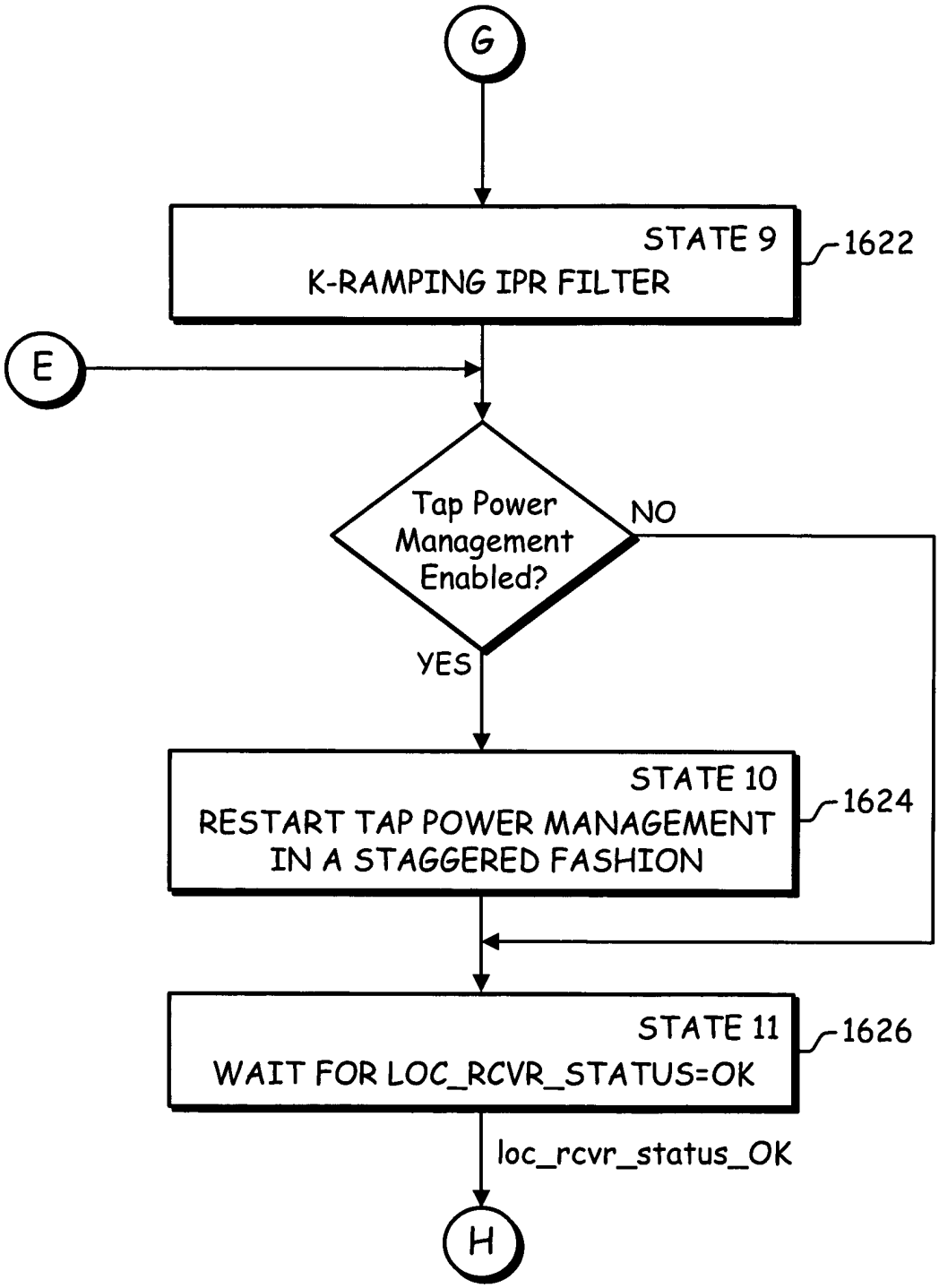

G
STATE 9
K-RAMPING IPR FILTER
1622
E
Tap Power Management Enabled?
NO
YES
STATE 10
RESTART TAP POWER MANAGEMENT IN A STAGGERED FASHION
1624
STATE 11
WAIT FOR LOC_RCVR_STATUS=OK
1626
loc_rcvr_status_OK
H

FIG. 16F

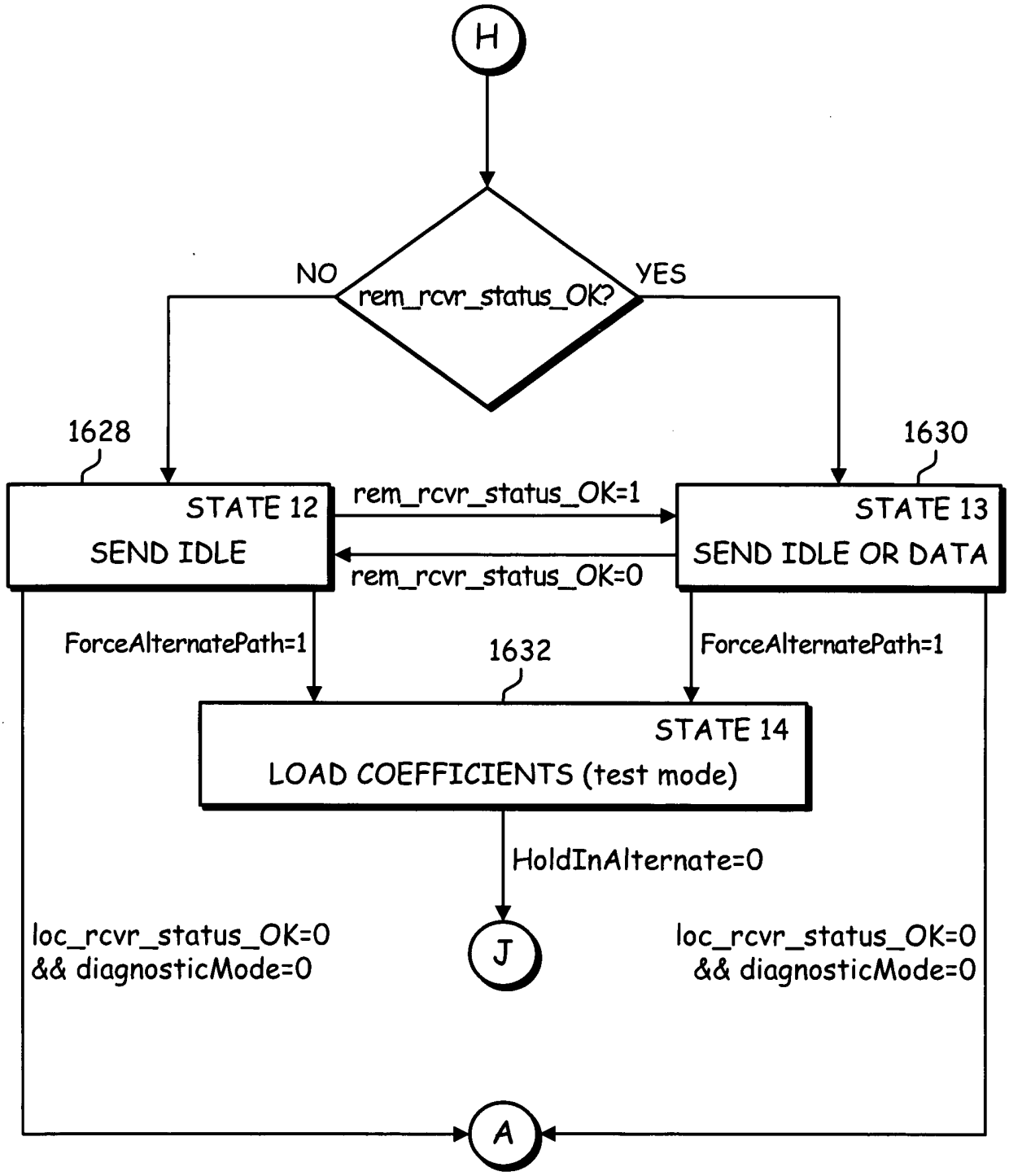

H
NO
rem_rcvr_status_OK?
YES
1628
1630
STATE 12
SEND IDLE
rem_rcvr_status_OK=1
rem_rcvr_status_OK=0
STATE 13
SEND IDLE OR DATA
ForceAlternatePath=1
1632
ForceAlternatePath=1
STATE 14
LOAD COEFFICIENTS (test mode)
HoldInAlternate=0
loc_rcvr_status_OK=0
&& diagnosticMode=0
J
loc_rcvr_status_OK=0
&& diagnosticMode=0
A

FIG. 16G

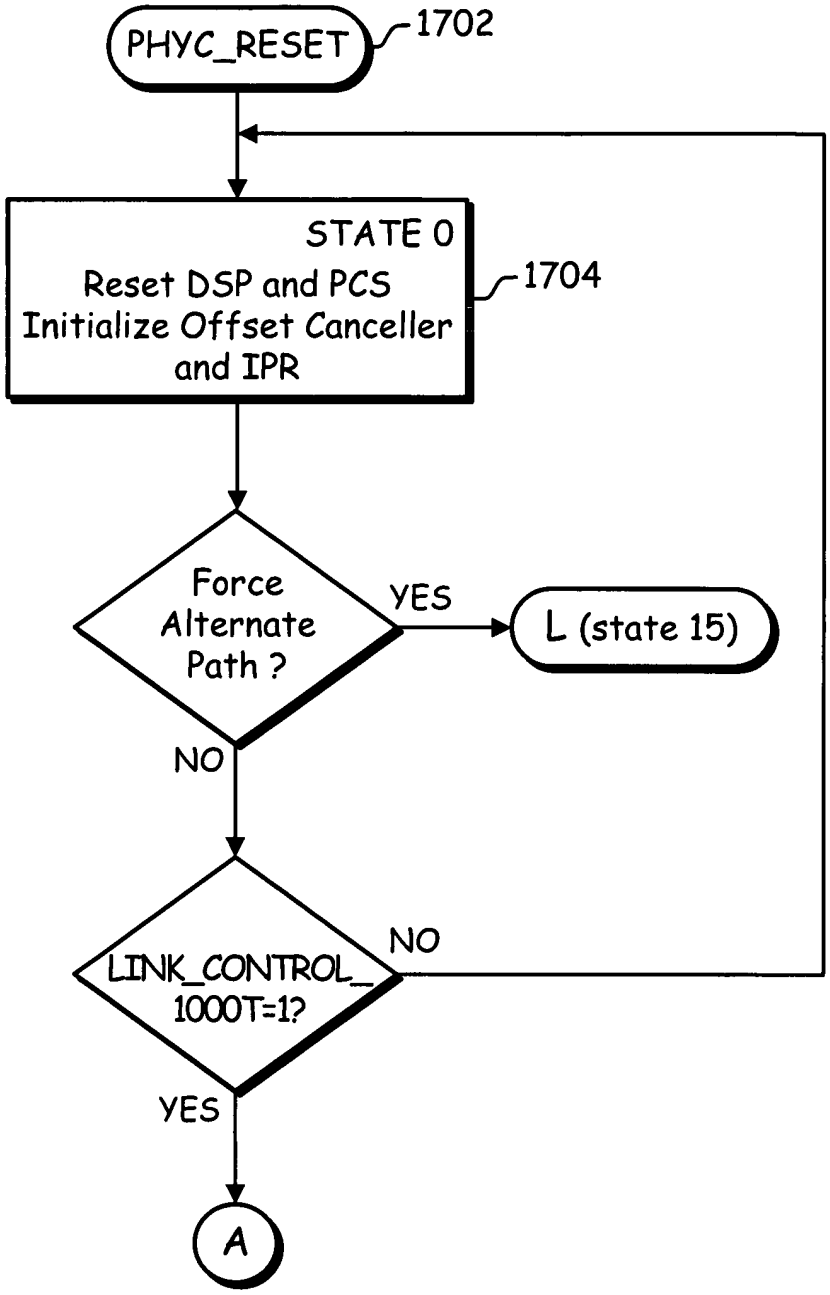

PHYC_RESET
1702
STATE 0
Reset DSP and PCS
Initialize Offset Canceller
and IPR
1704
Force
Alternate
Path ?
YES
L (state 15)
NO
LINK_CONTROL_
1000T=1?
NO
YES
A

FIG. 17A

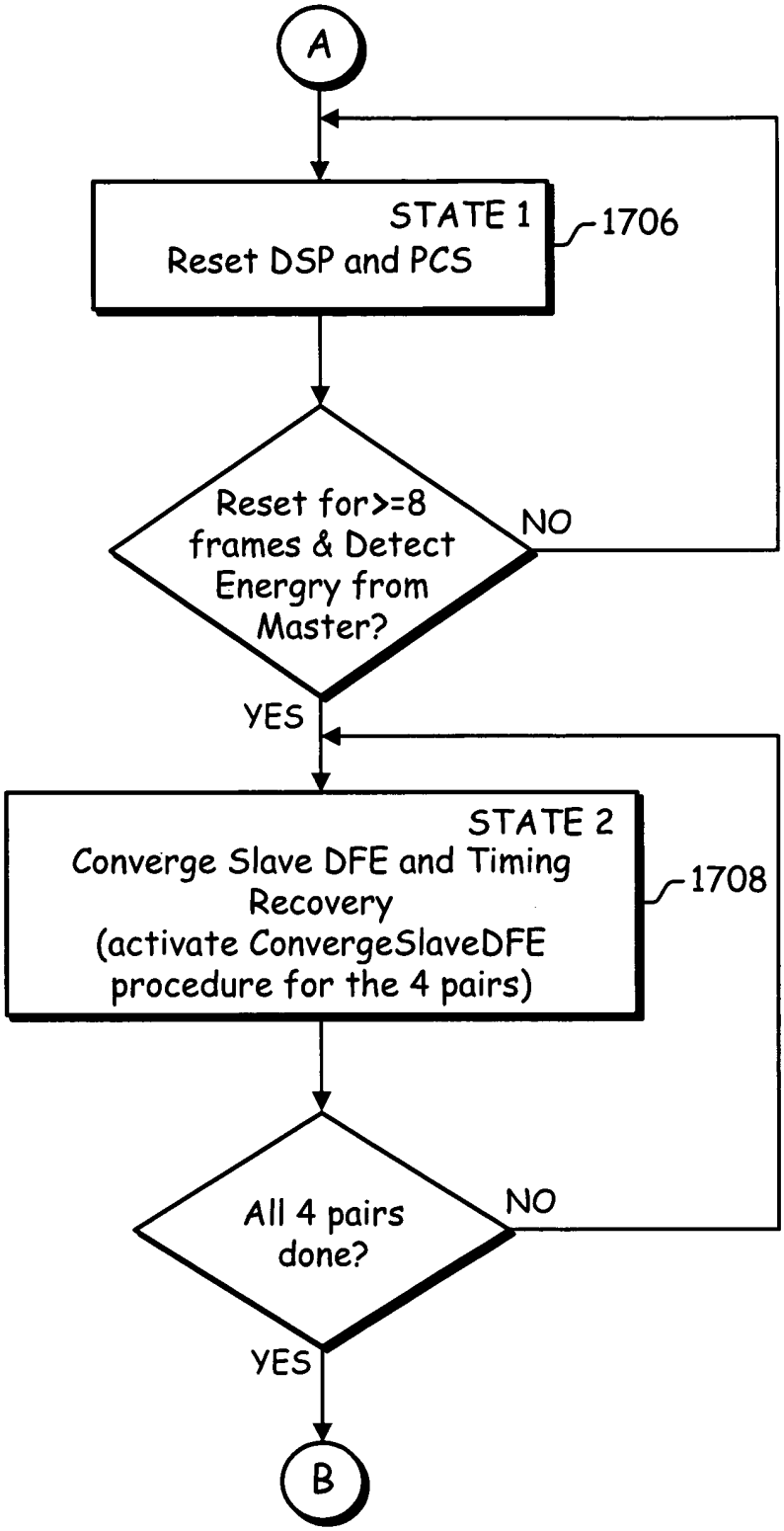

A
STATE 1
Reset DSP and PCS
1706
Reset for>=8 frames & Detect Energry from Master?
NO
YES
STATE 2
Converge Slave DFE and Timing Recovery (activate ConvergeSlaveDFE procedure for the 4 pairs)
1708
All 4 pairs done?
NO
YES
B

FIG. 17B

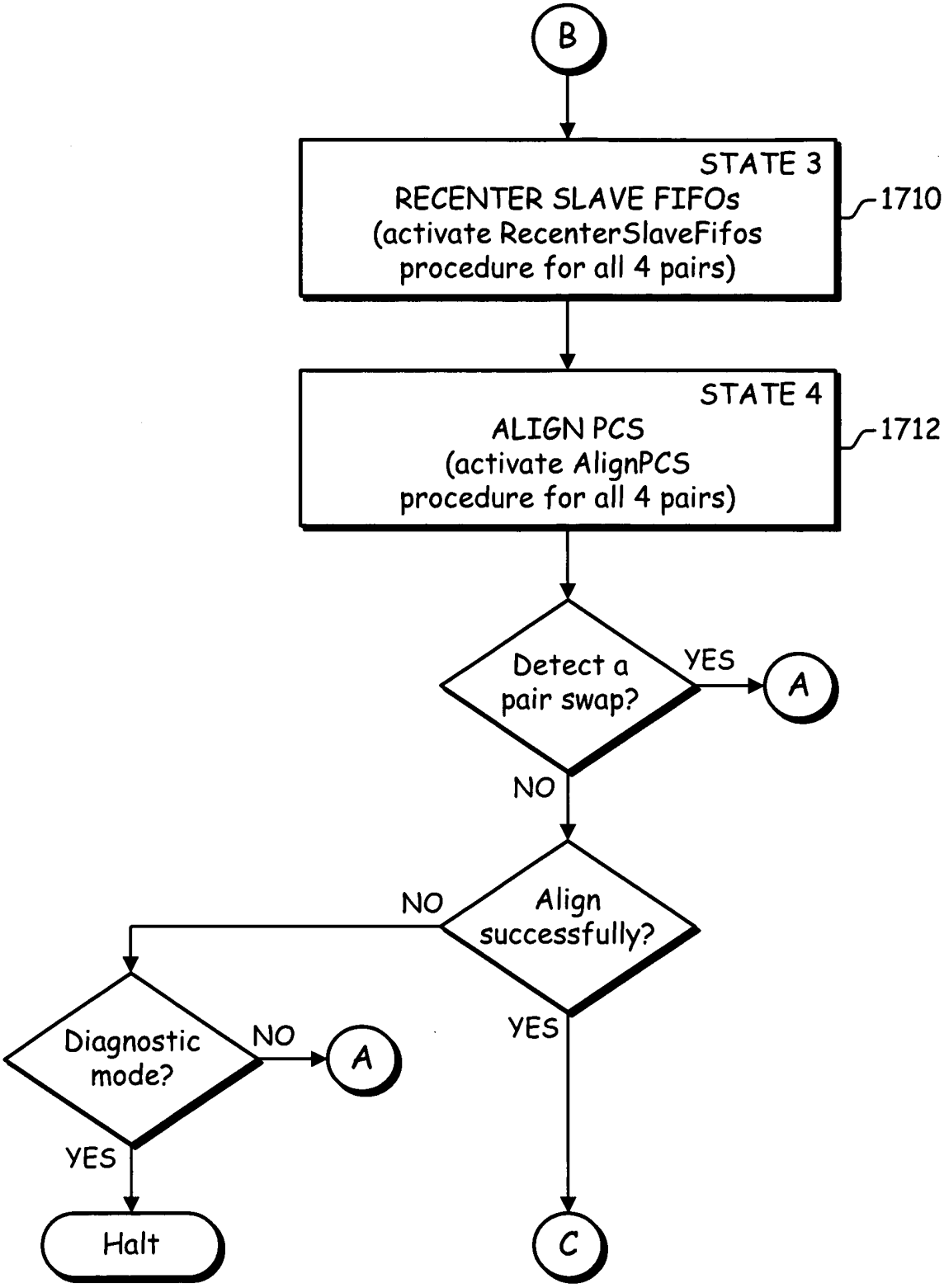

B
STATE 3
RECENTER SLAVE FIFOs
(activate RecenterSlaveFifos
procedure for all 4 pairs)
1710
STATE 4
ALIGN PCS
(activate AlignPCS
procedure for all 4 pairs)
1712
Detect a
pair swap?
YES
A
NO
Align
successfully?
NO
YES
Diagnostic
mode?
NO
A
YES
Halt
C

FIG. 17C

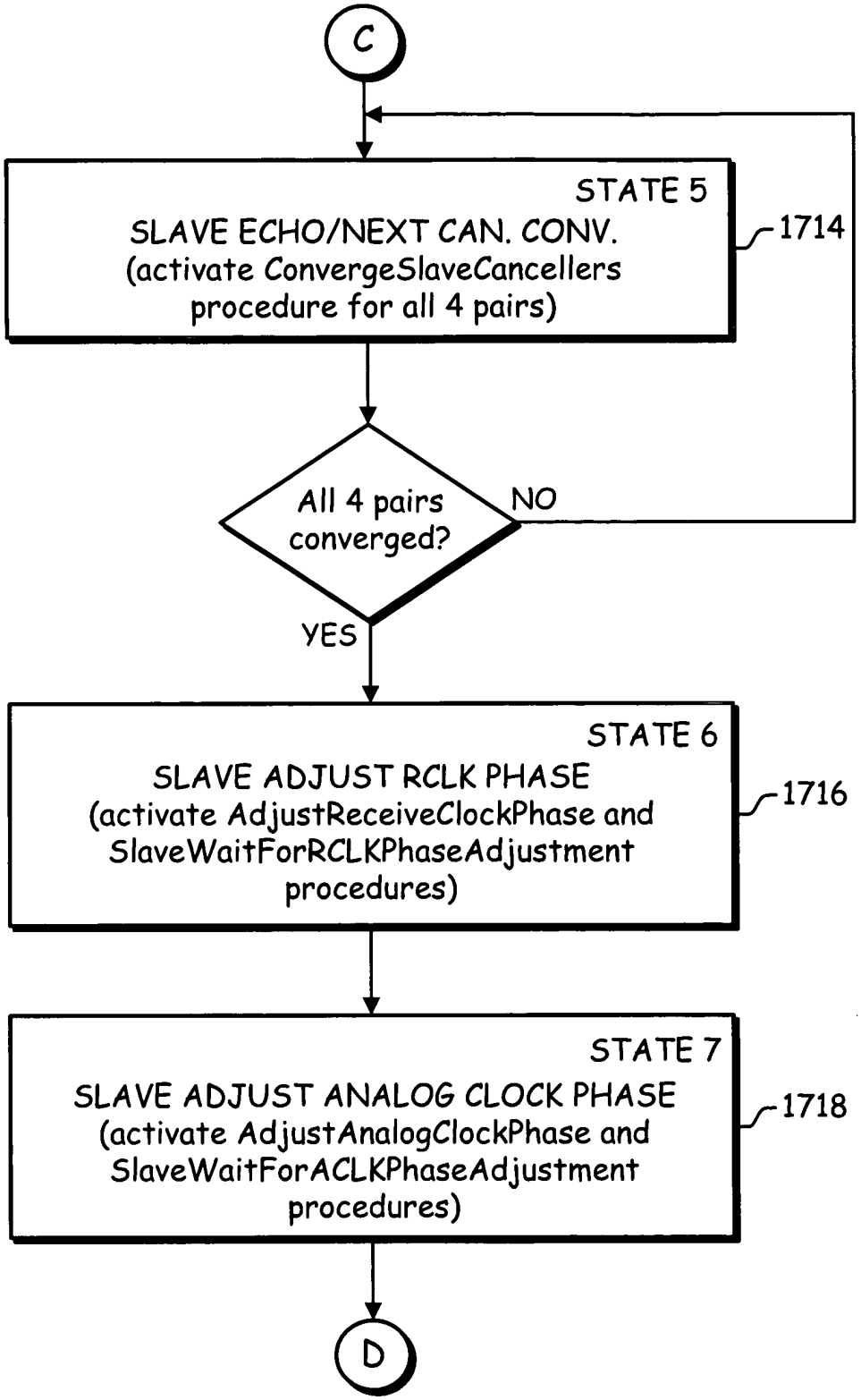

C
STATE 5
SLAVE ECHO/NEXT CAN. CONV.
(activate ConvergeSlaveCancellers
procedure for all 4 pairs)
1714
All 4 pairs
converged?
NO
YES
STATE 6
SLAVE ADJUST RCLK PHASE
(activate AdjustReceiveClockPhase and
SlaveWaitForRCLKPhaseAdjustment
procedures)
1716
STATE 7
SLAVE ADJUST ANALOG CLOCK PHASE
(activate AdjustAnalogClockPhase and
SlaveWaitForACLKPhaseAdjustment
procedures)
1718
D

FIG. 17D

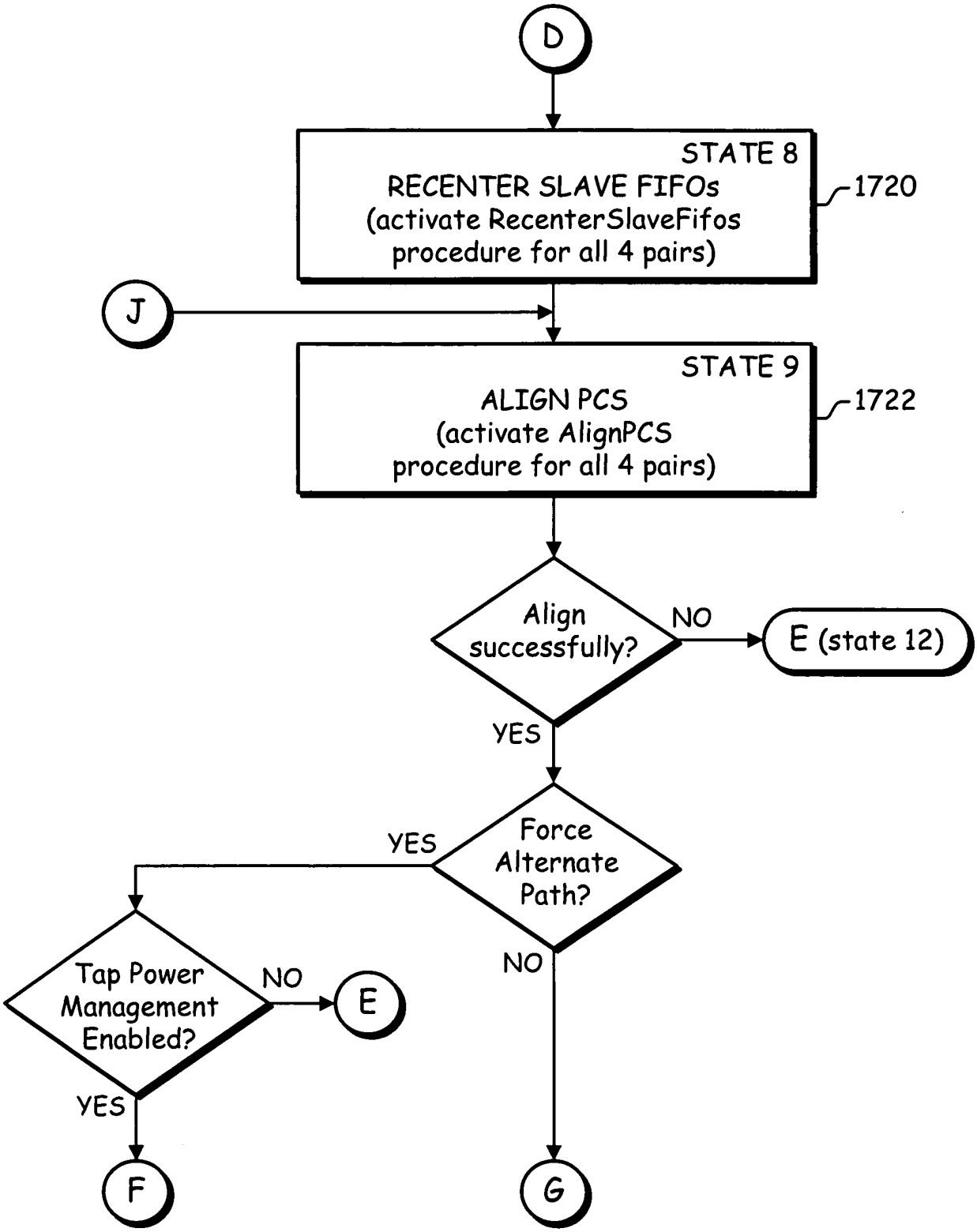

D
STATE 8
RECENTER SLAVE FIFOs
(activate RecenterSlaveFifos
procedure for all 4 pairs)
1720
J
STATE 9
ALIGN PCS
(activate AlignPCS
procedure for all 4 pairs)
1722
Align
successfully?
NO
E (state 12)
YES
Force
Alternate
Path?
YES
NO
Tap Power
Management
Enabled?
NO
E
YES
F
G

FIG. 17E

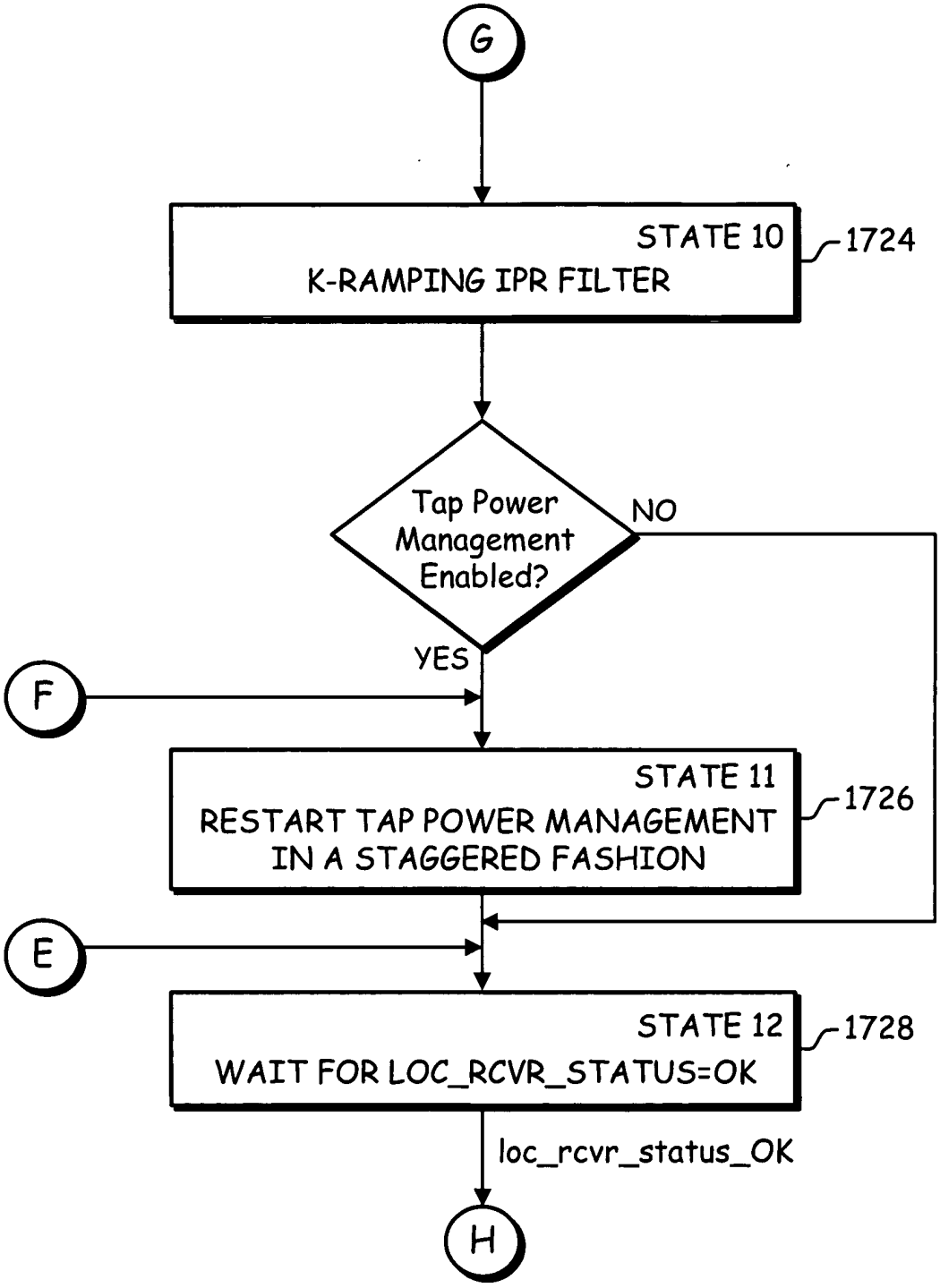

G
STATE 10
K-RAMPING IPR FILTER
1724
Tap Power Management Enabled?
NO
YES
F
STATE 11
RESTART TAP POWER MANAGEMENT IN A STAGGERED FASHION
1726
E
STATE 12
WAIT FOR LOC_RCVR_STATUS=OK
1728
loc_rcvr_status_OK
H

FIG. 17F

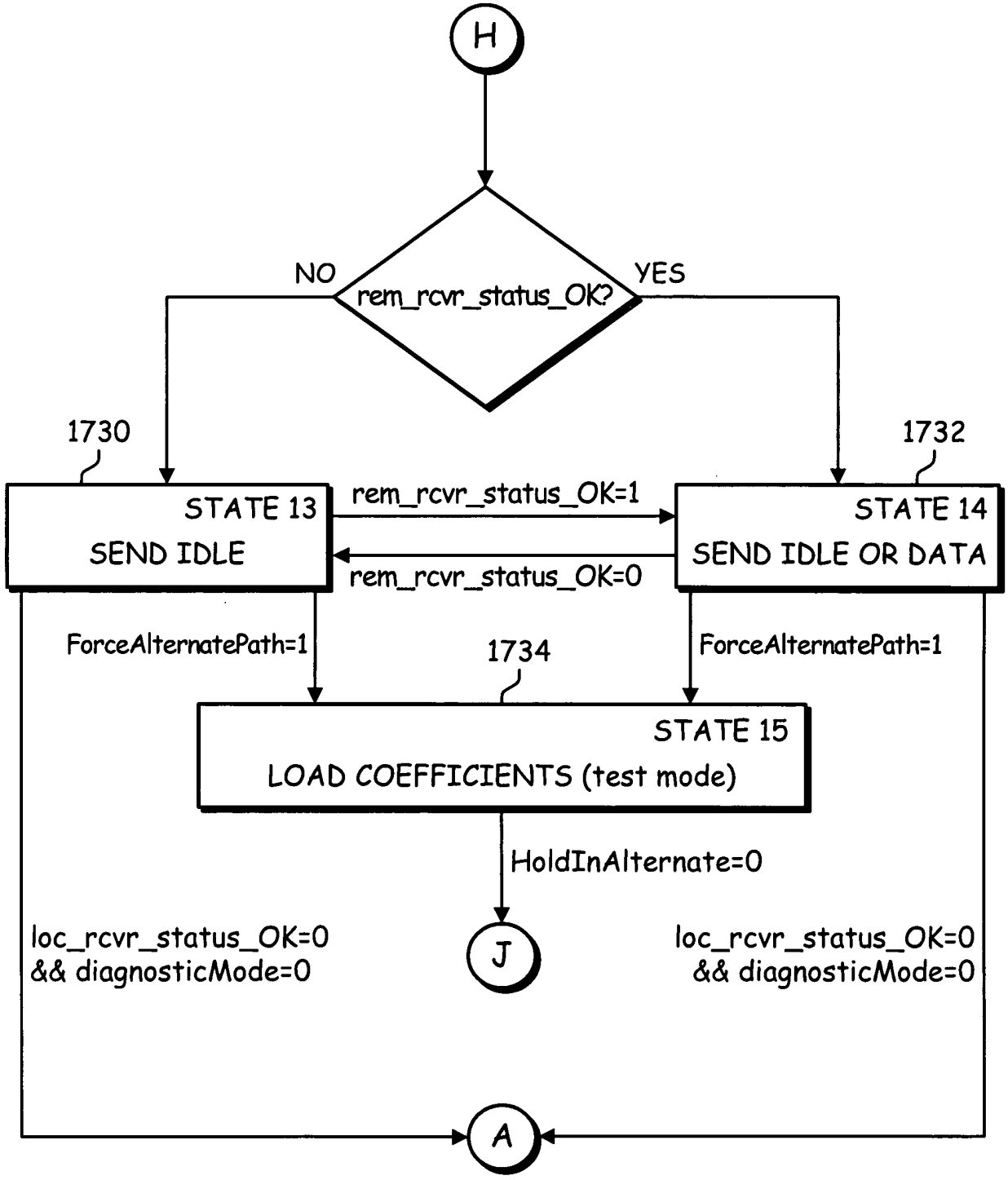

H
NO
rem_rcvr_status_OK?
YES
1730
1732
STATE 13
SEND IDLE
rem_rcvr_status_OK=1
rem_rcvr_status_OK=0
STATE 14
SEND IDLE OR DATA
ForceAlternatePath=1
1734
ForceAlternatePath=1
STATE 15
LOAD COEFFICIENTS (test mode)
HoldInAlternate=0
loc_rcvr_status_OK=0
&& diagnosticMode=0
J
loc_rcvr_status_OK=0
&& diagnosticMode=0
A

FIG. 17G

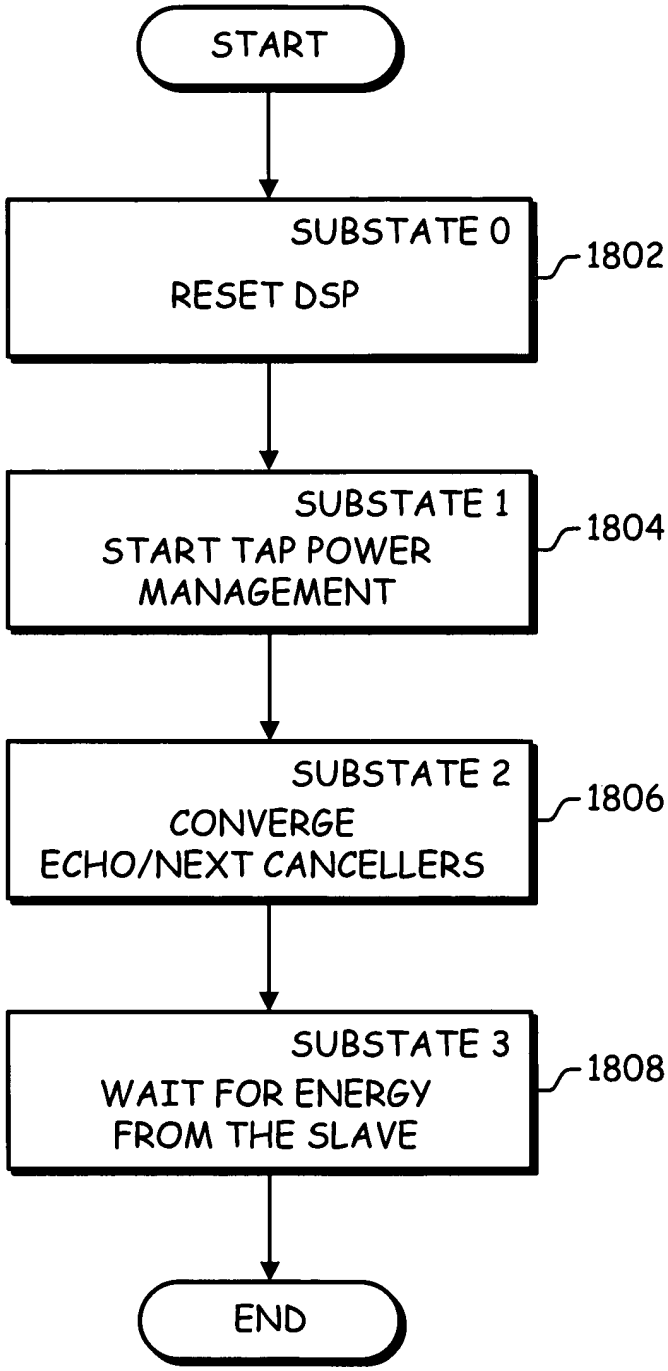

START
SUBSTATE 0
RESET DSP
1802
SUBSTATE 1
START TAP POWER MANAGEMENT
1804
SUBSTATE 2
CONVERGE ECHO/NEXT CANCELLERS
1806
SUBSTATE 3
WAIT FOR ENERGY FROM THE SLAVE
1808
END

FIG. 18

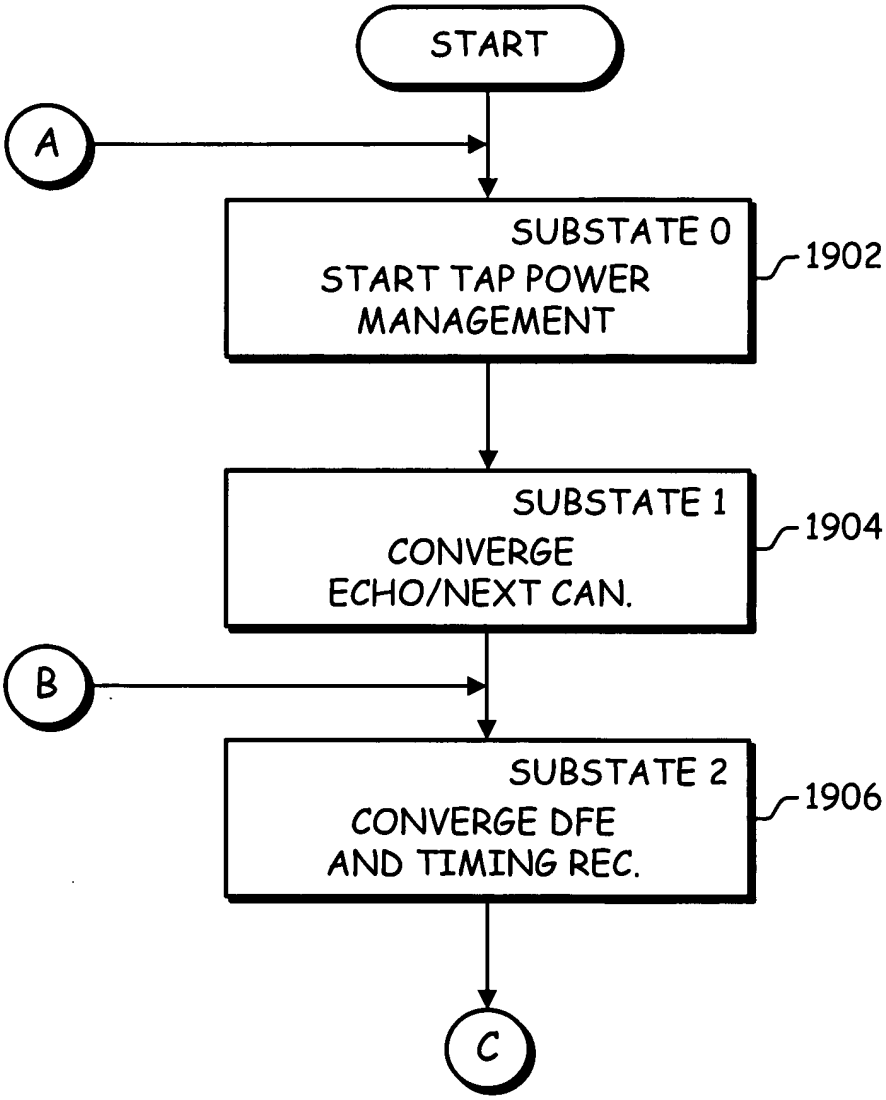

START
A
SUBSTATE 0
START TAP POWER MANAGEMENT
1902
SUBSTATE 1
CONVERGE ECHO/NEXT CAN.
1904
B
SUBSTATE 2
CONVERGE DFE AND TIMING REC.
1906
C

FIG. 19A

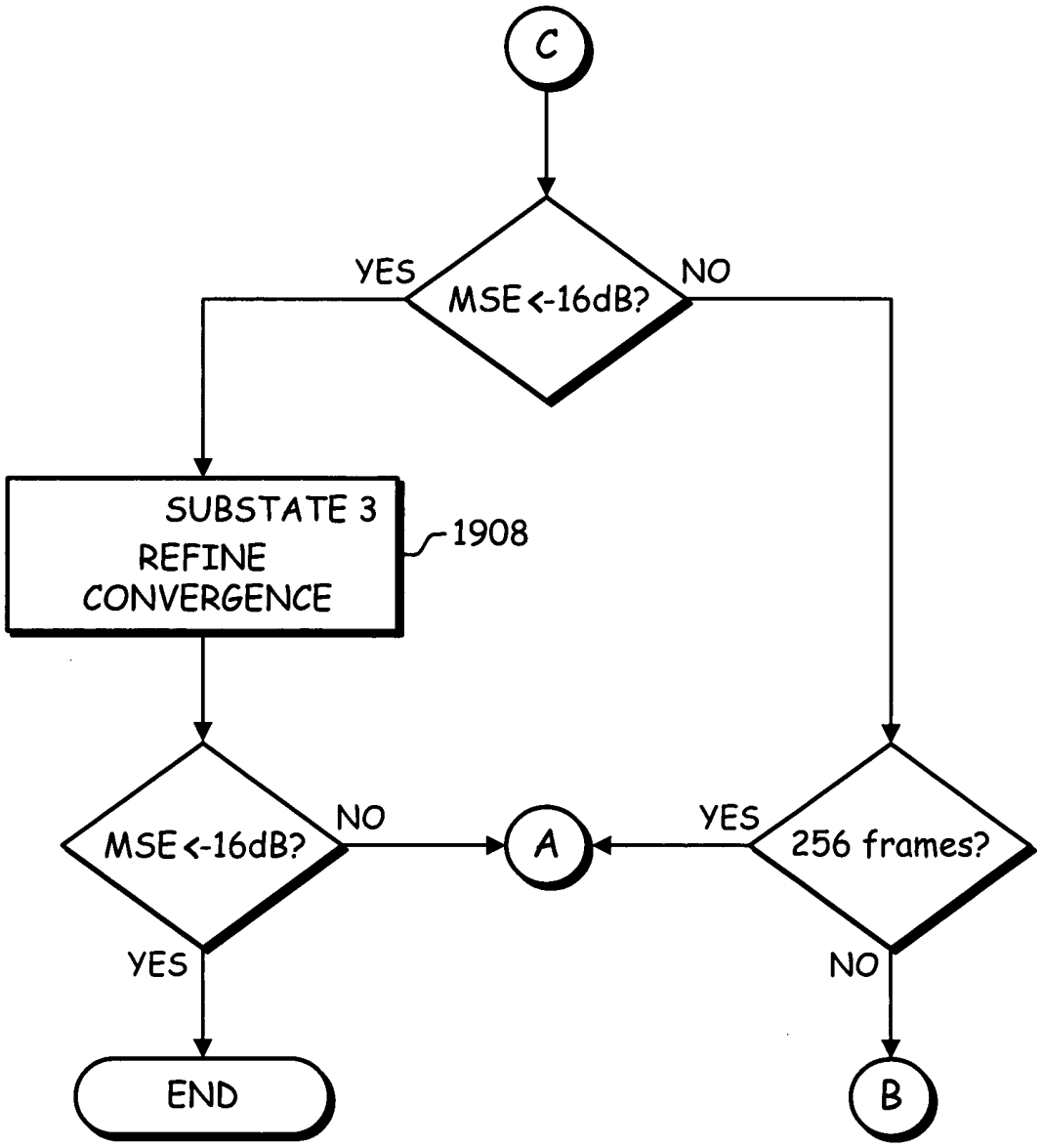

C
YES
MSE<-16dB?
NO
SUBSTATE 3
REFINE
CONVERGENCE
1908
MSE<-16dB?
NO
A
YES
256 frames?
YES
NO
END
B

FIG. 19B

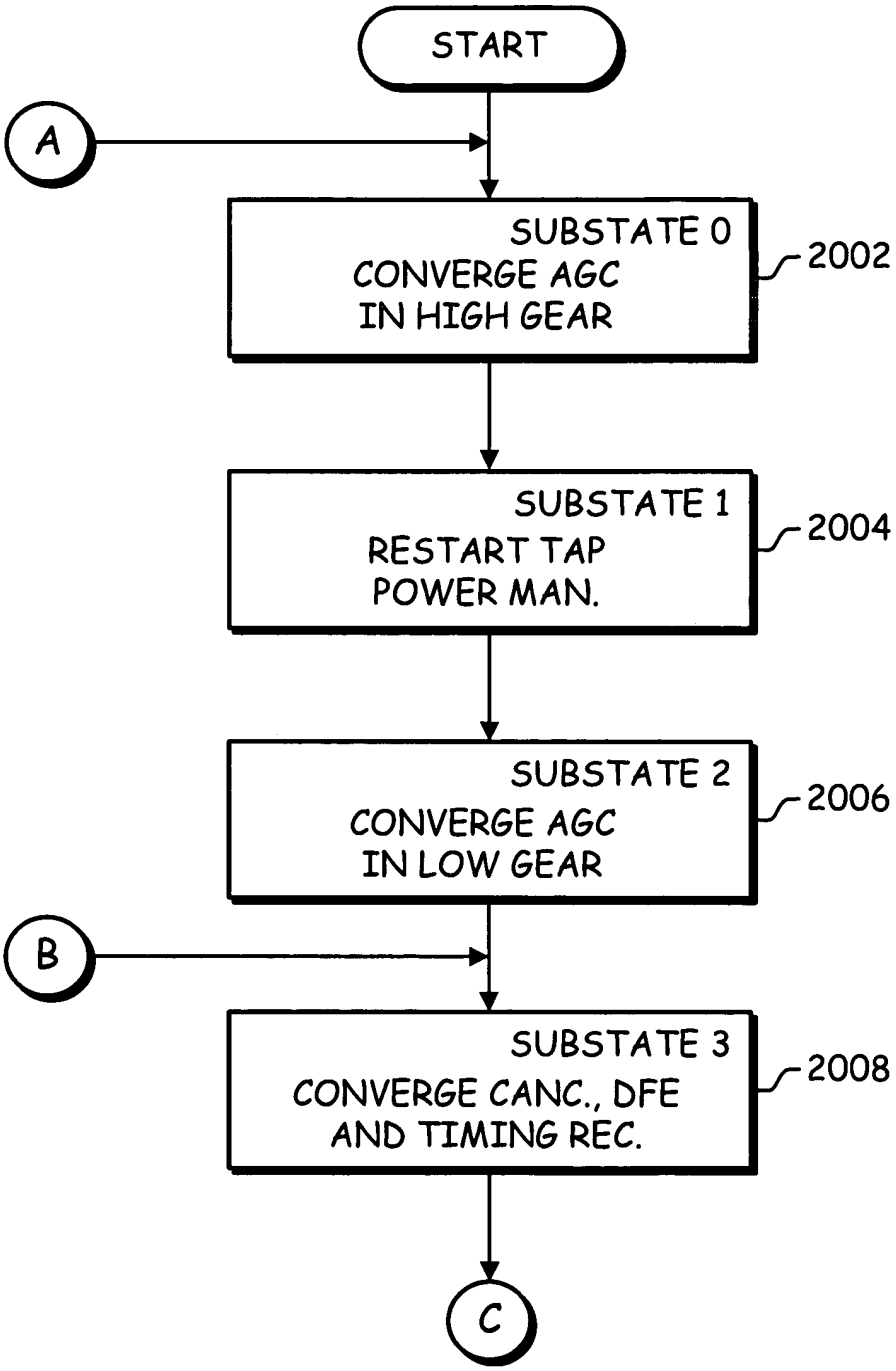

START
A
SUBSTATE 0
CONVERGE AGC
IN HIGH GEAR
2002
SUBSTATE 1
RESTART TAP
POWER MAN.
2004
SUBSTATE 2
CONVERGE AGC
IN LOW GEAR
2006
B
SUBSTATE 3
CONVERGE CANC., DFE
AND TIMING REC.
2008
C

FIG. 20A

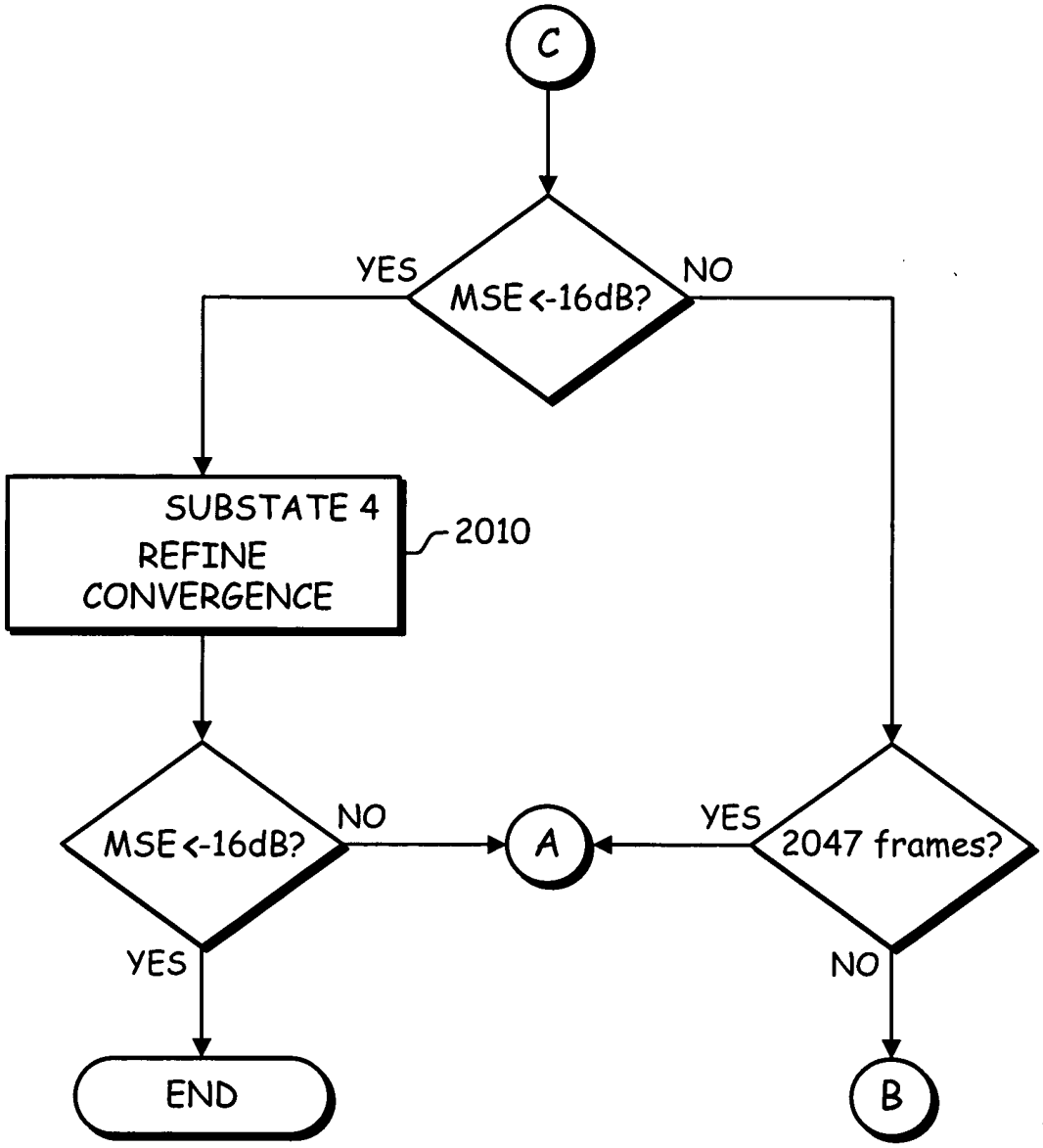

C
YES
MSE<-16dB?
NO
SUBSTATE 4
REFINE
CONVERGENCE
2010
MSE<-16dB?
NO
A
YES
2047 frames?
YES
NO
END
B

FIG. 20B

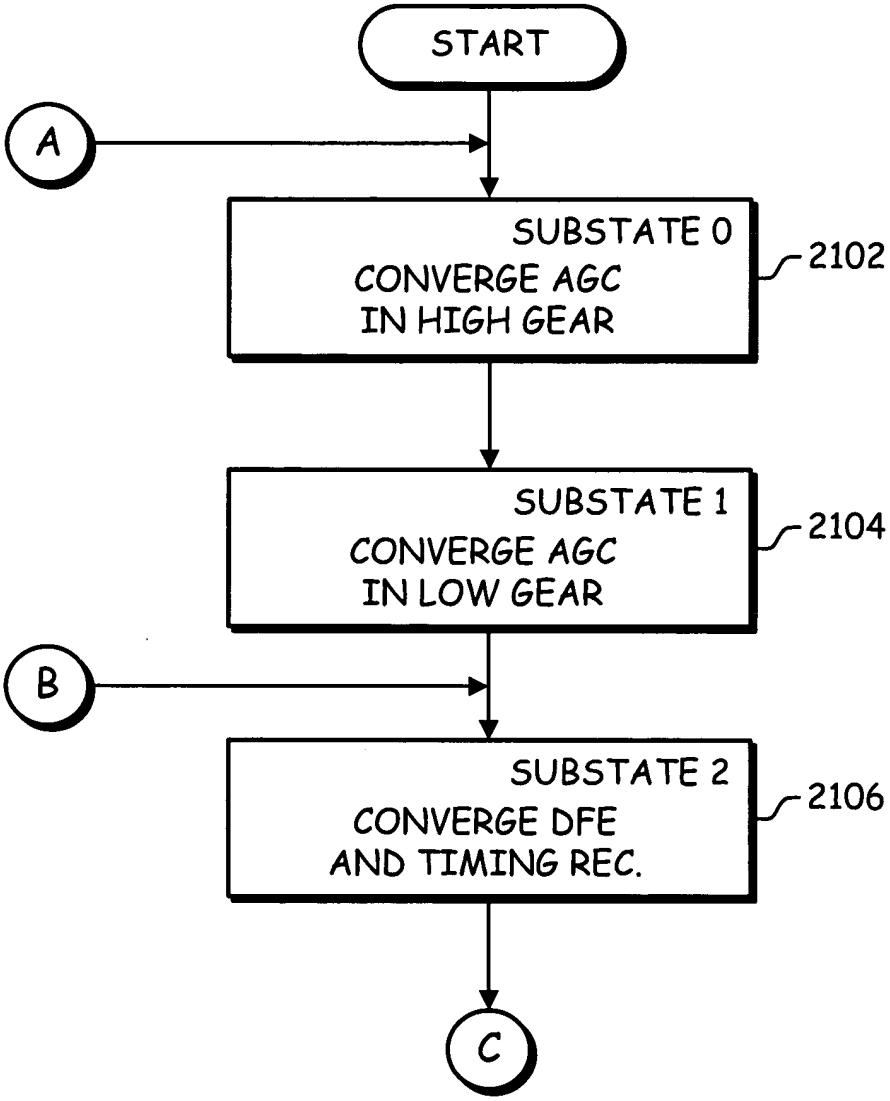

START
A
SUBSTATE 0
CONVERGE AGC
IN HIGH GEAR
2102
SUBSTATE 1
CONVERGE AGC
IN LOW GEAR
2104
B
SUBSTATE 2
CONVERGE DFE
AND TIMING REC.
2106
C

FIG. 21A

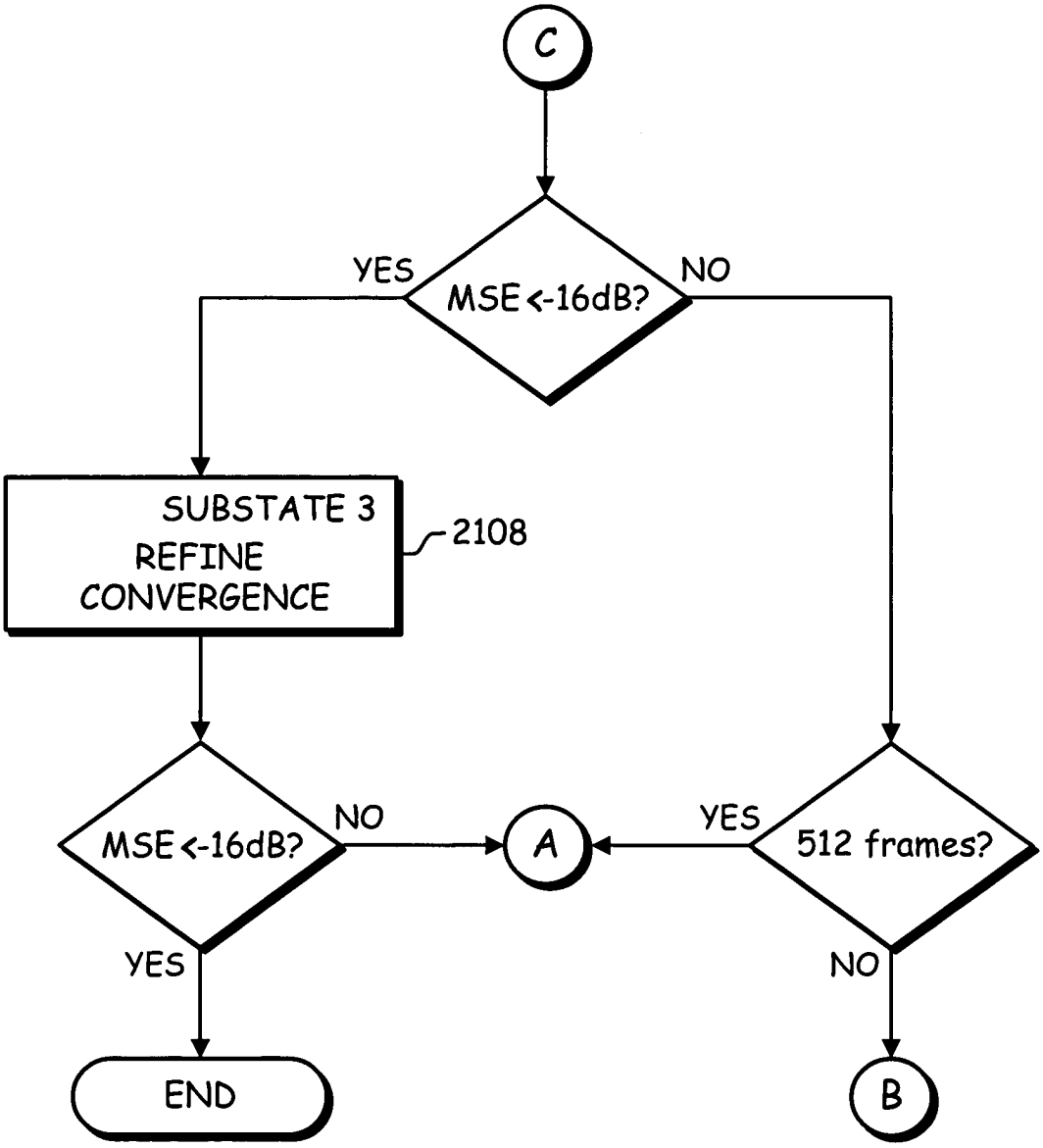

C
YES
MSE <-16dB?
NO
SUBSTATE 3
REFINE
CONVERGENCE
2108
MSE <-16dB?
NO
A
YES
512 frames?
YES
NO
END
B

FIG. 21B

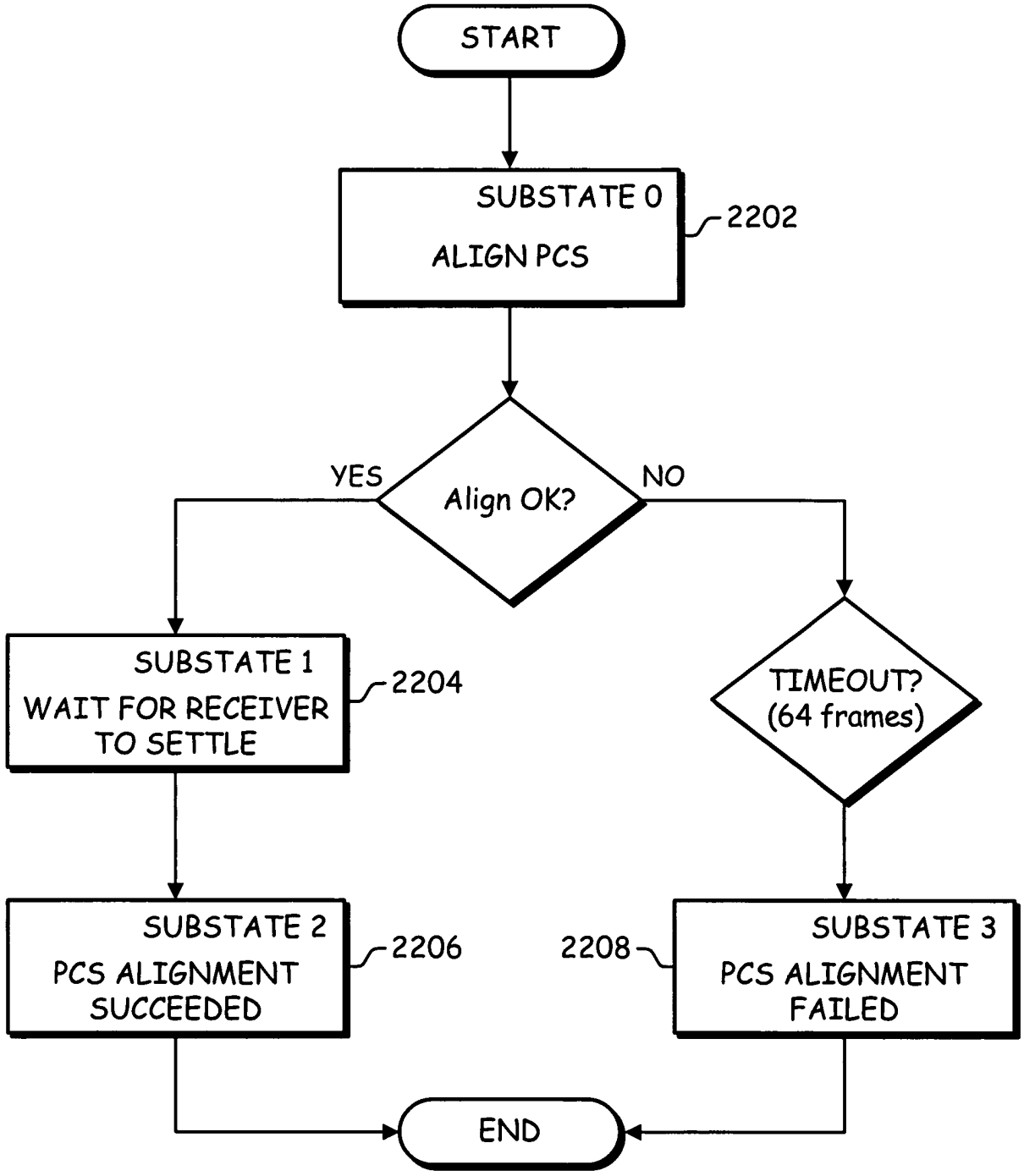

START
SUBSTATE 0
ALIGN PCS
2202
Align OK?
YES
NO
SUBSTATE 1
WAIT FOR RECEIVER TO SETTLE
2204
TIMEOUT? (64 frames)
SUBSTATE 2
PCS ALIGNMENT SUCCEEDED
2206
2208
SUBSTATE 3
PCS ALIGNMENT FAILED
END

FIG. 22

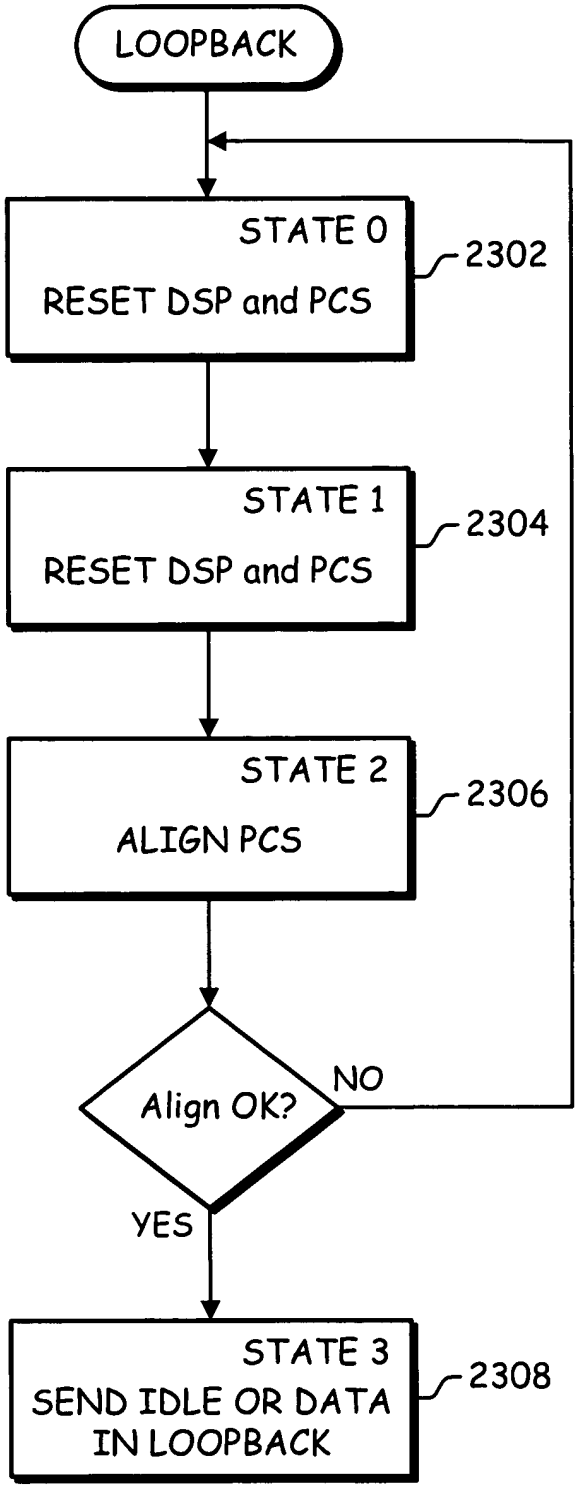

LOOPBACK
STATE 0
RESET DSP and PCS
2302
STATE 1
RESET DSP and PCS
2304
STATE 2
ALIGN PCS
2306
Align OK?
NO
YES
STATE 3
SEND IDLE OR DATA
IN LOOPBACK
2308

FIG. 23

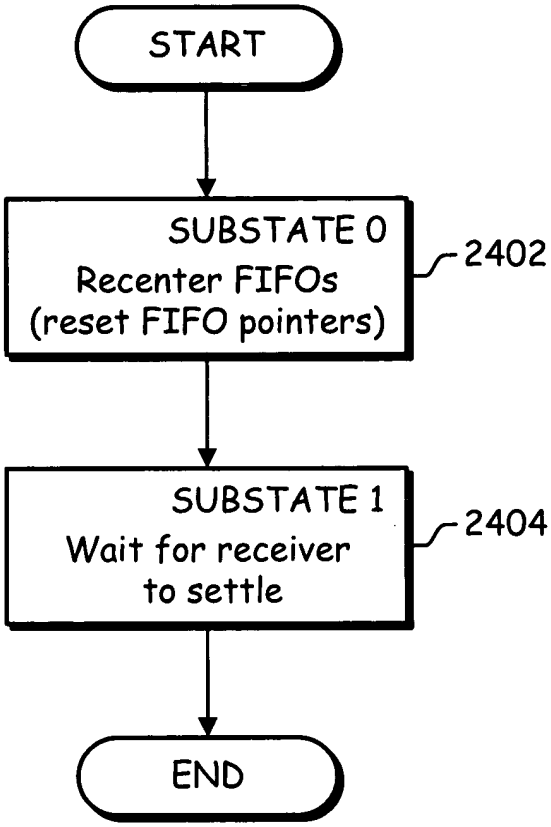

START
SUBSTATE 0
Recenter FIFOs
(reset FIFO pointers)
2402
SUBSTATE 1
Wait for receiver
to settle
2404
END

FIG. 24

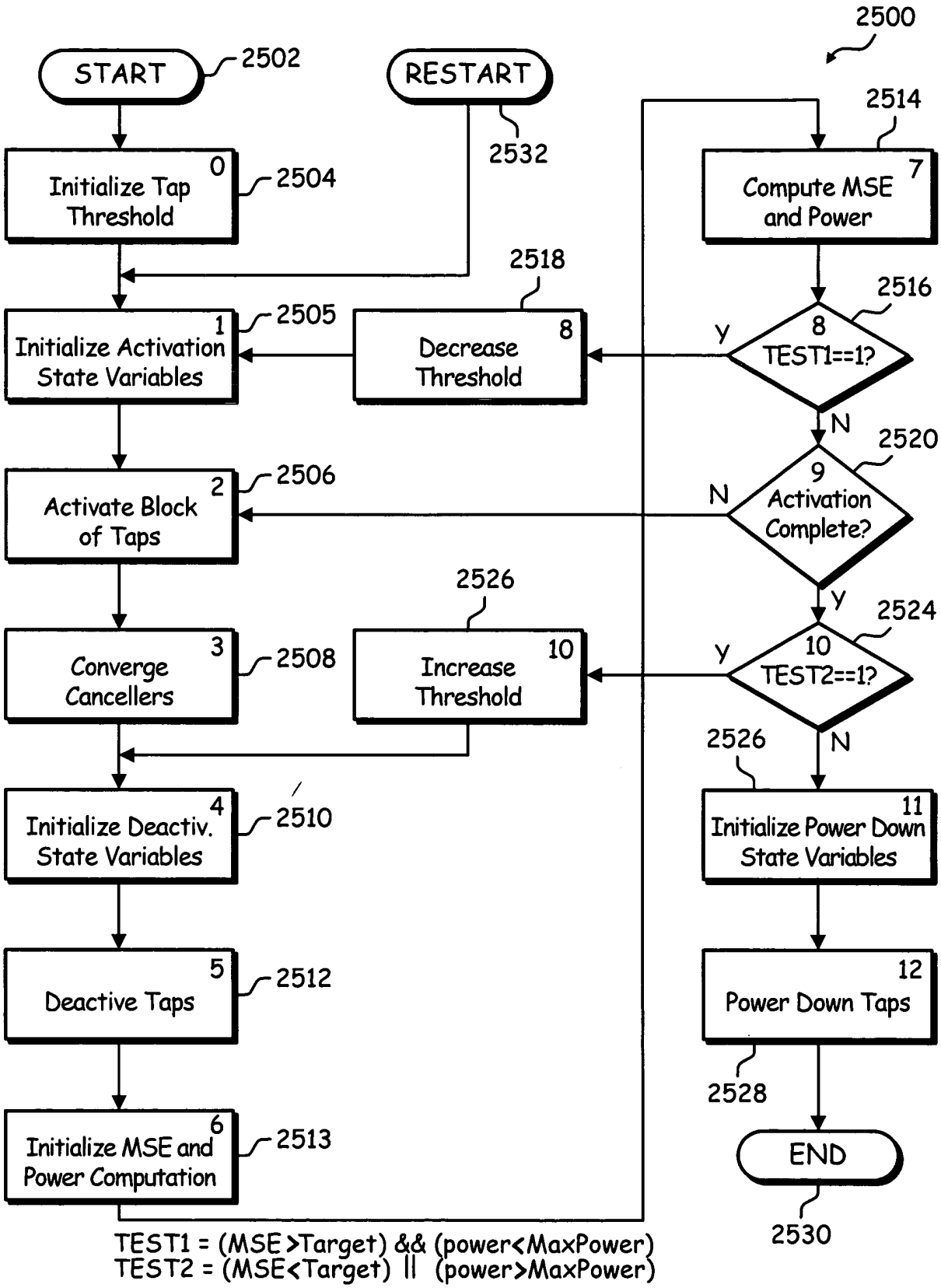

2500
START
2502
RESTART
2532
2514
Initialize Tap Threshold
0
2504
Compute MSE and Power
7
2518
2516
Initialize Activation State Variables
1
2505
Decrease Threshold
8
8 TEST1==1?
y
N
2520
Activate Block of Taps
2
2506
9 Activation Complete?
N
y
2526
2524
Converge Cancellers
3
2508
Increase Threshold
10
10 TEST2==1?
y
2526
N
Initialize Deactiv. State Variables
4
2510
Initialize Power Down State Variables
11
Deactive Taps
5
2512
Power Down Taps
12
2528
Initialize MSE and Power Computation
6
2513
END
2530
TEST1 = (MSE>Target) && (power<MaxPower)
TEST2 = (MSE<Target) || (power>MaxPower)

FIG. 25

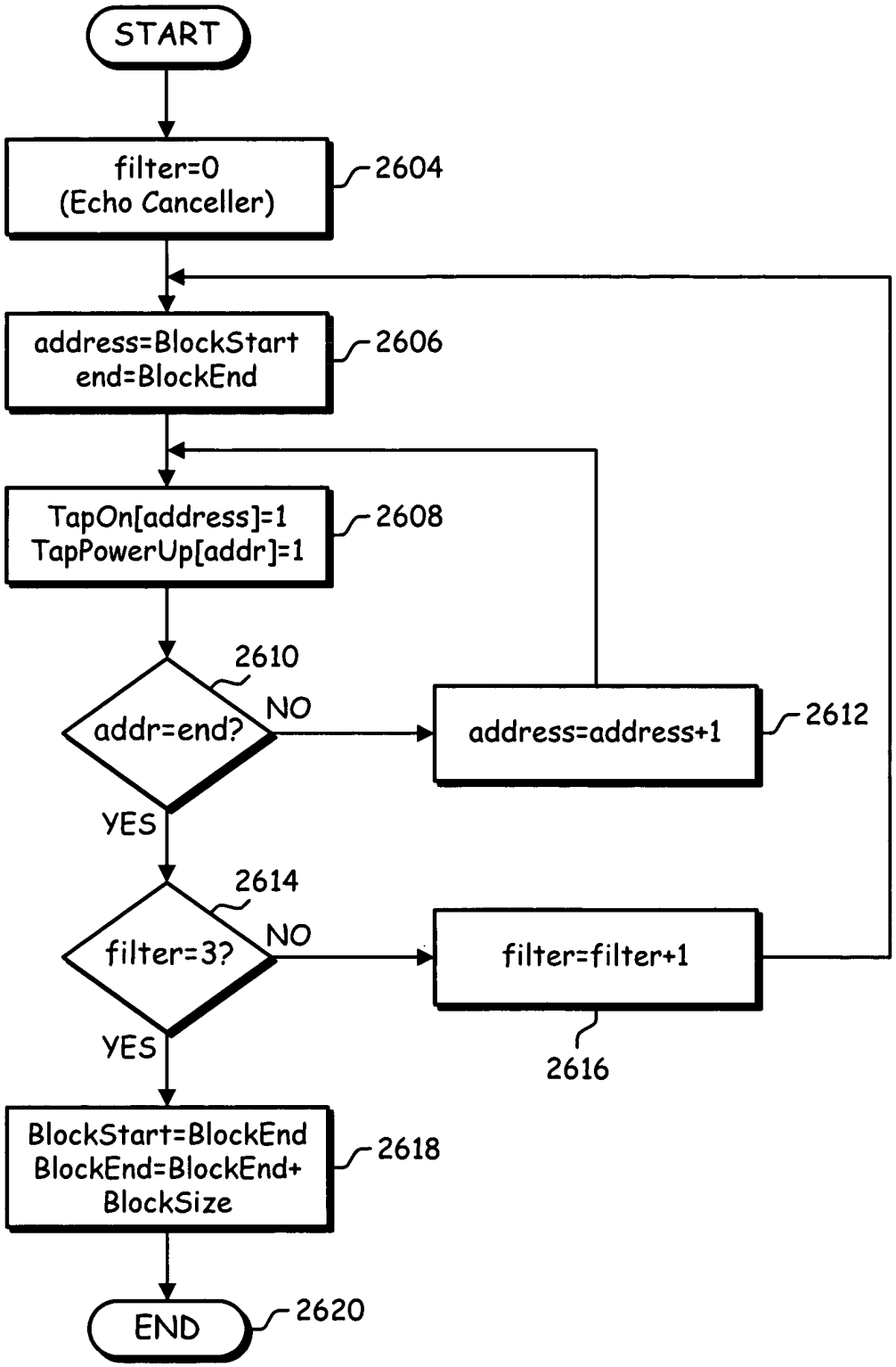

START
filter=0
(Echo Canceller)
2604
address=BlockStart
end=BlockEnd
2606
TapOn[address]=1
TapPowerUp[addr]=1
2608
2610
addr=end?
NO
address=address+1
2612
YES
2614
filter=3?
NO
filter=filter+1
2616
YES
BlockStart=BlockEnd
BlockEnd=BlockEnd+
BlockSize
2618
END
2620

FIG. 26

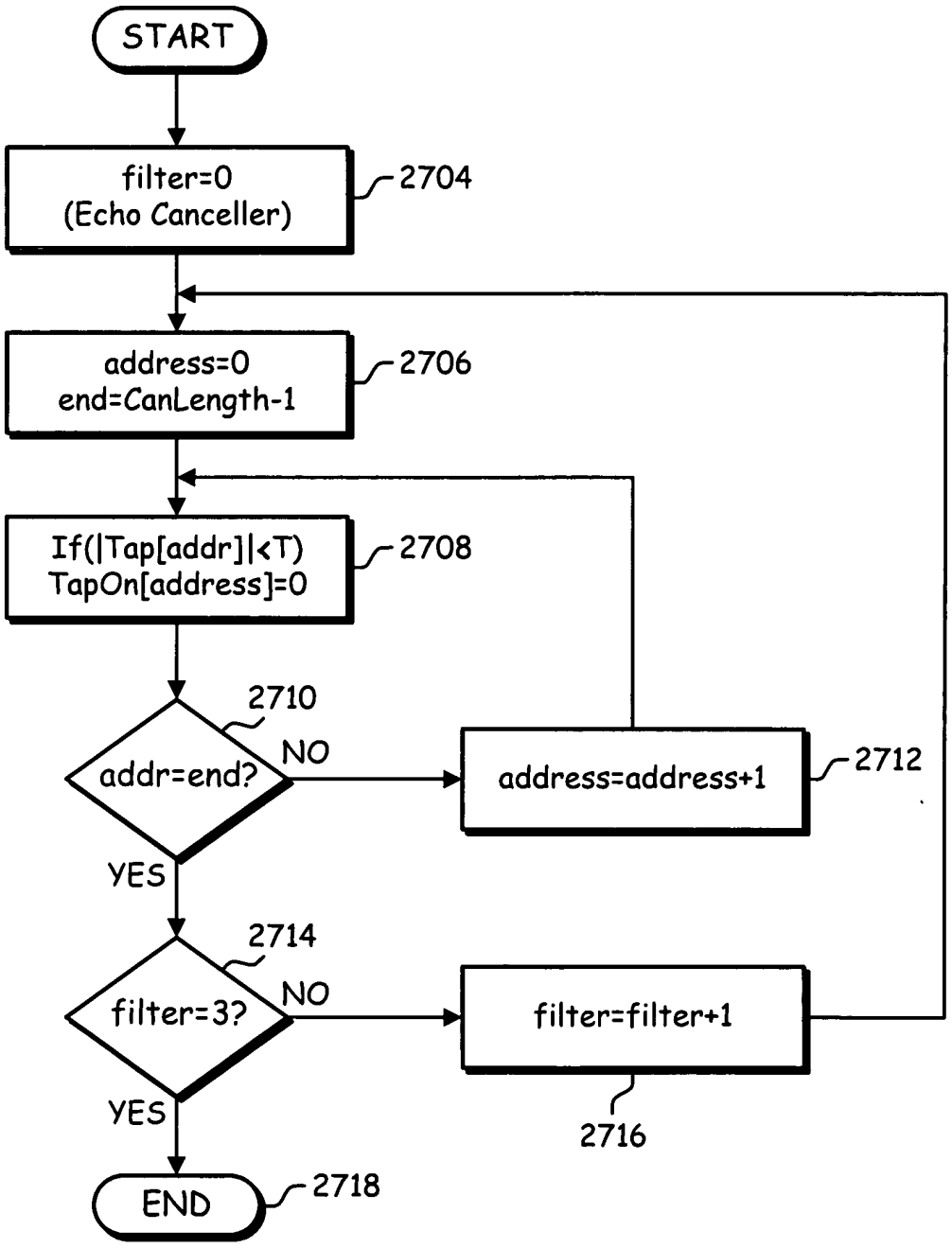

START
filter=0
(Echo Canceller)
2704
address=0
end=CanLength-1
2706
If(|Tap[addr]|<T)
TapOn[address]=0
2708
2710
addr=end?
NO
address=address+1
2712
YES
2714
filter=3?
NO
filter=filter+1
2716
YES
END
2718

FIG. 27

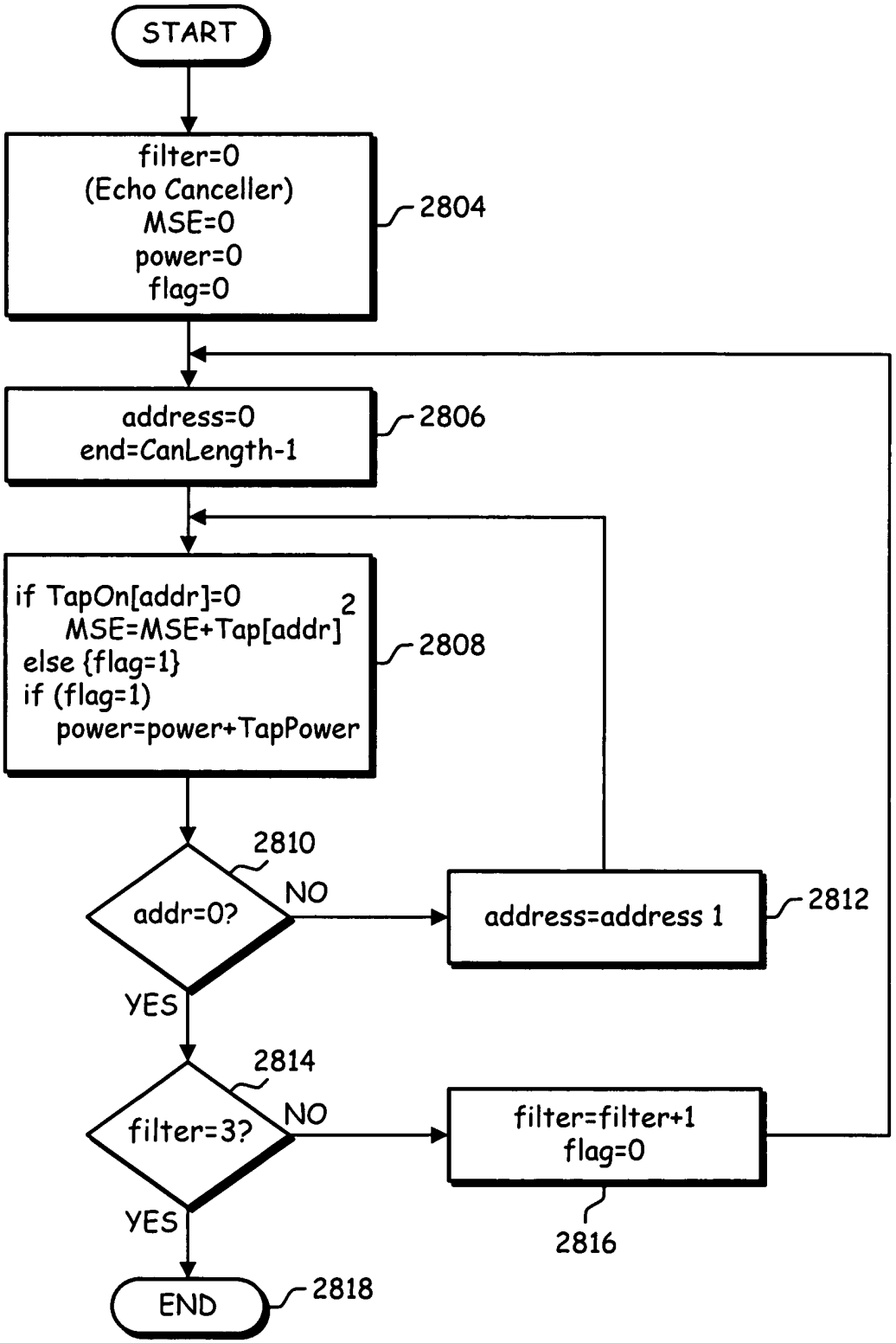

START
filter=0
(Echo Canceller)
MSE=0
power=0
flag=0
2804
address=0
end=CanLength-1
2806
if TapOn[addr]=0
MSE=MSE+Tap[addr]2
else {flag=1}
if (flag=1)
power=power+TapPower
2808
2810
addr=0?
NO
address=address 1
2812
YES
2814
filter=3?
NO
filter=filter+1
flag=0
2816
YES
END
2818

FIG. 28

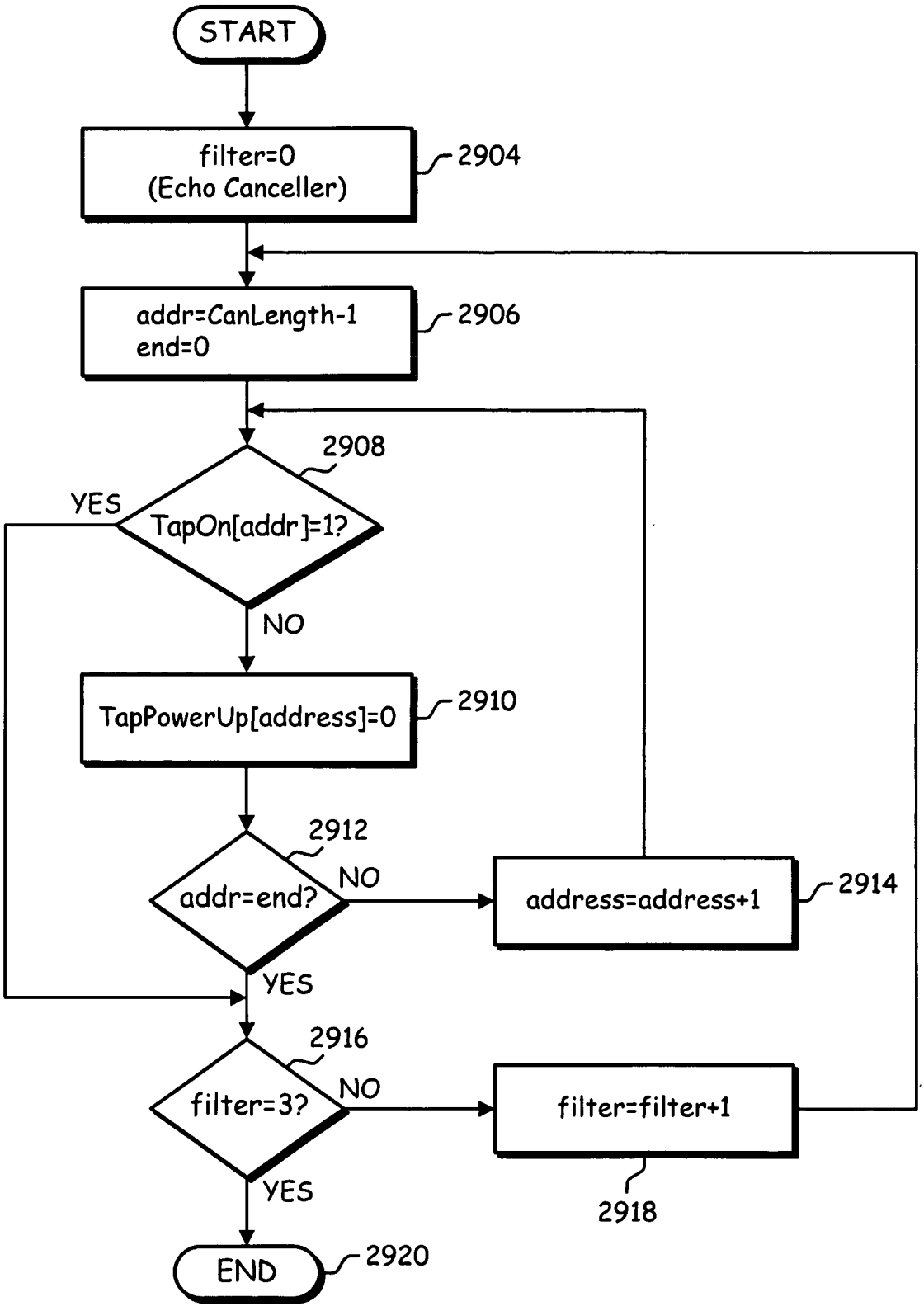

START
filter=0
(Echo Canceller)
2904
addr=CanLength-1
end=0
2906
2908
YES
TapOn[addr]=1?
NO
TapPowerUp[address]=0
2910
2912
addr=end?
NO
address=address+1
2914
YES
2916
filter=3?
NO
filter=filter+1
2918
YES
END
2920

FIG. 29